## HFSS\_3DLGS\_2019R3\_EN\_ WS3.1\_OctSpiral

HFSS 3D Layout Getting Started WS3.1



### On-Chip Octagonal Spiral Inductor

This workshop sets up and analyzes an octagonal spiral inductors using the ANSYS HFSS 3D Layout environment.

The following topics are covered in this example:

- Concept of equivalent inductance and return path
- Setting up vias
- Defining ports for simulation
- Defining output variables for L and Q-factor
- Analyzing the effect on inductance and quality factor using several Solver options

(DC Thickness, Solve Inside)

Starting file for this workshop:

OnChip\_OctSpiralL0.aedtz



Finished spiral inductor including via solderballs up to the BRD layer that is not shown here.



#### On Chip Spiral Inductor - Workshop Outline

#### Outline of steps done in this workshop:

- Open archive file of octagonal spiral missing two vias
- Add two vias including modifying the padstack definition.
- Add long vertical ground return current paths with the solderball files
- Add two ports
- Adjust *HFSS Extents* to define the substrate and bounding box.
- Add HFSS Solution Setup for finite element method simulation
- Add *Output Variables* for Inductance and Quality Factor
- Simulate and View Results
- Copy Data in Reports and then copy design for solve inside
- Set HFSS settings to solve inside for design **Spiral\_Ind\_SolveInside**
- Compare results from the two different simulations

OnChip\_OctSpiralL0.aedtz OnChip\_OctSpiralL1.aedt

OnChip\_OctSpiralL2.aedt OnChip\_OctSpiralL2.aedt

OnChip\_OctSpiralL2.aedt OnChip\_OctSpiralL3.aedt OnChip\_OctSpiralL3.aedt OnChip\_OctSpiralL4.aedt OnChip\_OctSpiralL4.aedt



#### Launching AEDT - HFSS 3D Layout - Restore Archive

Launch the ANSYS Electronics Desktop (AEDT) to access HFSS 3D Layout ...

- In Microsoft Windows, click the Microsoft Start button, select *Programs > ANSYS EM Suite 20XXRY > ANSYS Electronics Desktop* A new *Project1* appears under the *Project Manager*.
- In the *Ribbon*, in the Desktop tab, select the icon for *Restore Archive*.





A windows browser will appear ...



#### Restore Archive to OnChip\_OctSpiralLO.aedt

- Browse to the training files and restore the file **OnChip\_OctSpiralL0.aedtz**
- Restore the file **OnChip\_OctSpiralLO.aedt** to a working directory.

EDT Archive to Rest	tore			$\times$	Project File Res	tore Location			×
Look in:	WS3.1_Octagor	al_Spiral	• 🔁 📸 🐨 ▼		Save in:	WS3.1_Octago	nal_Spiral		
Quick access Desktop Libraries This PC	Name	^ iralL0.aedtz	Type ANSYS Electronics	Date modified 11/20/2019 12:0	Quick access Desktop Libraries This PC	Name	^ No items match	Type your search.	
	File name: Files of type: View Archive Contended	OnChip_OctSpiralL0.aedtz ANSYS Electronics Desktop Archi	▼ ve File Types (*. ▼	Open Cancel		<ul> <li>File name:</li> <li>Save as type:</li> <li>Overwrite existin</li> <li>Open project after</li> </ul>	OnChip_OctSpiralL0.aedt ANSYS Electronics Desktop Pr g files er restoring	roject File (*.aedt)	<ul> <li>Save</li> <li>Cancel</li> </ul>



#### Spiral Inductor Layout

This initial spiral inductor has the dielectric padding and extents specified. The blue line around the spiral sets both the dielectric boundary and the airbox simulation space.

This initial spiral inductor is missing two vias, which will extend vertically up to a plane that completes the ground return current path.

This initial spiral inductor is missing two ports.



This *Display Default* view shows the rectangle, on the **BRD** level, to which the *Extents* conform.





#### Concept of Equivalent Inductance





#### Concept of Equivalent Inductance in Our Spiral Inductor

HFSS calculates the equivalent Inductance of a net:

- Inductive and capacitive effects will be included.
- Loop inductance has more physical meaning than partial inductance.
- A close current loop must be formed in order to accurately simulate the loop inductance.

We'll construct very long(vertically) vias that create this return path through the BRD layer.





- 1. It is always recommended to include the real return path in a structure being simulated.
- 2. If it is not possible to add the real return path, we have to assume where the return path is going to be.



## Spiral Geometry Overview





#### Set Active Layer to AP - OnChip\_OctSpiralLO.aedt

There are two ways to set the active drawing layer:

- 1. From the toolbar, locate the toolbar for the Active Layer, From the pull-down, select the layer **AP**
- 2. In the Layout tab, use the *Active Layer* pull down



We're preparing to draw vias.

 Set *Display* to *Sketch*.



#### Drawing a Via - Snap to Center of Circle

- Prepare to draw a Via:
  - Make sure that *Snap object center* is enabled. (Layout tab)
  - Shift to *Top* view
  - Set to Display Sketch.
- Draw the via in the center of the circle:
  - Click on the icon for Draw Via.
  - Move the cursor to the circle on the spiral.
  - Look for another circle to indicate snap to the circle center and click when the via is snapped.

Indication

of snap





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Default size of via

(diameter): 1mm

#### Modifying Via: Set Start and Stop Layers





## Modifying a Via: Modifying Padstack - Open Select Definition Window

In the *Properties* tab for the via ...

- Click on the Value PlanarEMVia, to bring up the Select Definition window.
  - In the *Select Definition* window for the Padstacks
  - Scroll down to select *Template 1mm/0.5mm* and click *Edit Padstack*.
  - In the Select Definition window click on the Edit Padstack ... button to bring up the Edit Padstack Definition window.

Properties	무
Name	Value
Туре	Via
LockPosition	
Name	via_2028
Net	
Padstack Definition	PlanarEMVia
Padstack Usage	
Start Layer	AP
Stop Layer	Metal6

- Search Parameters	Librari	es 🔽 Sho	w Project defin
	[sys]	Padstacks	
Search			
A Name	Location	Origin	Has Hole?
Round 2mm/1mmPin0deg	SysLibrary	Padstacks	Yes
Round 3.176mm SMT	SysLibrary	Padstacks	
Round 3.176mmPin0deg SMT	SysLibrary	Padstacks	
Round 3.22mmPin0deg SMT	SysLibrary	Padstacks	
Round 3.938mm SMT	SysLibrary	Padstacks	
Round 3.938mmPin0deg SMT	SysLibrary	Padstacks	
Round 5.08mm SMT	SysLibrary	Padstacks	
Round 5.08mmPin0deg SMT	SysLibrary	Padstacks	
Round 6.096mm SMT	SysLibrary	Padstacks	
Round 6.096mmPin0deg SMT	SysLibrary	Padstacks	
Round/T 1mm/0.8/0.5mm	SysLibrary	Padstacks	Yes
Square/Round 1mm/0.5mm	SysLibrary	Padstacks	Yes
Template 1mm/0.5mm	SysLibrary	Padstacks	Yes
Template0 1mm/0.5mm	SysLibrary	Padstacks	Yes



## Edit Padstack Definition Window - OnChip\_OctSpiralLO.aedt

In the *Edit Padstack Definition* window

- 1. General settings:
  - Name: Solder\_Template
- 2. Hole settings:
  - Shape: Circle
  - Diameter: 15um
- 3. Solderball
  - Shape: None
- 4. In *Layers* section, click on the button to highlight the layer
  - Pad settings:
    - > Shape: Circle
    - Diameter: 25um
  - Anti pad settings:
    - Shape: None
  - Thermal pad settings:
    - Shape: None
  - Connection point settings:
    - Direction: None
- Click the OK button to close this window and then to close the Select Definition window.





## Copying the Top Via to the Bottom - OnChip\_OctSpiralL1.aedt

In the layout, with the top via selected:

- Select the menu item *Edit > Copy*
- Select the menu item *Edit > Paste*
- Move the cursor to the lower circle and click after it snaps to the object.



Properties	
Name	Value
Туре	Via
LockPosition	
Name	via_2029
Net	
Padstack Definition	Solder_Template
Padstack Usage	
Start Layer	AP
Stop Layer	Metal5
Backdrill Top	
Backdrill Bottom	
OverrideHoleDiam	
HoleDiameter	15

- In the *Properties* window for the bottom via change:
- 1. Start Layer: **AP**
- 2. Stop Layer: *Metal5* 
  - Save the project as OnChip\_SpiralL1.aedt.



#### View Both Vias with Z-Stretch - OnChip\_OctSpiralL1.aedt

In the layout, the vertical dimension can be stretched for better viewing using *View > Stretch Z...* 



**Ansys** 



#### Selecting the Via in the Circle - Display Sketch

Properties	000000000000000000000000000000000000000	무 ×	
Name	Value	Unit	
Туре	circle		
Name	circle_1666		
LockPosition			
PlacementLayer	AP		
Net			
Negative			
Center	-0.245434793105	. mm	
Radius	0.015	mm	

roperties	~~~~	Ψ×
Name	Value	Unit
Туре	Via	
LockPosition		
Name	via_2028	
Net		
Padstack Definition	Solder_Template	
Padstack Usage		
Start Layer	AP	
Stop Layer	Metal6	
Backdrill Top		
Backdrill Bottom		

In the top-down view, it is easy to point at the via and select the circle instead. One can verify what is selected by referring to the *Properties*.

One good way to pick out and select a particular object, positioned close to other objects, is to use *Display Sketch*. In this way we can point at and select exactly what we want. Then in *Properties* we can verify that we have selected what we want (the via in this case).



### Create Solderball Reference on Top Via 1

With one of the vias selected, in the *Properties* window:

In the *Padstack Usage* line, under *Value*, click on the button (which should show ellipses, three periods in a row), to bring up the *Padstack Usage and Definition* window.

Solder Ball properties are added to create the long vertical sections for the return path.

Name	Value
Туре	Via
LockPosition	
Name	via_2028
Net	
Padstack Definition	Solder_Template
Padstack Usage	
Start Layer	AP
Stop Layer	Metal6

Padstack Usage and Definition		
General   Name:   Solder_Template     Via material   Select   Plating percent:   0     Range   Through all layout layers   Begin at upper pad   End at lower pad   From upper to lower pad	Padstack range Solderball Start: AP  Stop: Metal6	initial view continued



## Padstack Usage and Definition Window - OnChip\_OctSpiralL1.aedt

In the *Padstack Usage and Definition* window

- Set Padstack Range:
  - Start: AP
  - End: Metal6
- Solderball:
  - Shape: Cylinder
  - Diameter: 12.5um
  - Connection Layer: BRD
- Click the OK button, which brings up the Apply Padstack Definition Changes window

... continued ...

adstack Usage and Def	inition						
General Name: Solder_Temple Via material Select Plating percent 0	Ate Hole Shape Diame	: Circle  ter: 15um	Padstack rang Start AP Stop: Met	ge ▼ al6 ▼	-Solo Sha Diar -Co La	Ierball pe: Cylinder neter: 12.5um solder pnnection yer: BRD	Backdrill Top Depth: None Diameter: 0 Bottom Depth: None Diameter: 0
Layers							Cross section view
Layout	Padstack	Pad	Anti pad	Thermal pad		Connect pt	<b>^</b>
BRD	xisiok	xolok	kolok	slokok		kokk	
AP	Default	circle (25um)	none	none		None	
RV	Default	circle (25um)	none	none		None	
Metal6	Default	circle (25um)	none	none		None	
Via5	xxxx	*AAX	xxxxx	Xolok		Xokok	
Metal5	skolok	skolok	kolok	Makak:		****	~
Default mapping				Padstac	k defin	ition data has changed	
- Layer settings	Antina	d	Thormal pad		Con	naction point	T op view
Shape: None		Nono -	Shape: Nor		Diro	ction: Nono	
Shape: None	Shape	: None 💌	Shape: Nor	12	Dire	ction: None	
							OK Cancel



# Finish Solderball Reference for Top Via 1

In the In *Apply Padstack definition* changes window...

- Select *Create new definition*
- Select Only this via or pin
- Click the **OK** button



Apply Padstack Definition Changes

Х

#### Create Solderball Reference on Top Via 2

With one of the vias selected, in the *Properties* window:

In the *Padstack Usage* line, under *Value*, click on the button (which should show ellipses, three periods in a row), to bring up the *Padstack Usage and Definition* window.

Solder Ball properties are added to create the long vertical sections for the return path.

Properties	
Name	Value
Туре	Via
LockPosition	
Name	via_2029
Net	
Padstack Definition	Solder_Template
Padstack Usage	
Start Layer	AP
Stop Layer	Metal5

Padstack Usage and Definition				
General Name: Solder_Template Via material Select Plating percent 0	Hole Shape: Circle Diameter: 15um Range C Through all layout layers C Begin at upper pad C End at lower pad From upper to lower pad	Padstack range Start: AP Stop: Metal5	Solderball Shape: None 💌	initial view continued

## Padstack Usage and Definition Window - OnChip\_OctSpiralL1.aedt

In the *Padstack Usage and Definition* window

- Set Padstack Range:
  - Start: AP
  - End: Metal6
- Solderball:
  - Shape: Cylinder
  - Diameter: 12.5um
  - Connection Layer: BRD
- Click the OK button, which brings up the Apply Padstack Definition Changes window

... continued ...

orel								
General			Padstack range			Solderball		Backdrill
Name: Solder_Template Shape:		Circle 💌	Start:	P 🔻	Sha	pe: Cylinder	•	Тор
Via material Select	Diamet	ter: 15um	Stop:	1etal5 💌	Diar	meter: 0.0125mm		Depth: None
ating percent: 0		e hrough all layout layers egin at upper pad nd at lower pad rom upper to lower pad			-Co La	solder onnection yer: BRD	<b>•</b>	Bottom Depth: None 💌 Diameter: 0
vers								Cross section view
Layout	Padstack	Pad	Anti pad	Thermal pa	Thermal pad		^	
RD *	okok:	skolok	skolak	holok		Xolok		
P C	Default	circle (25um)	none	none		None		
۲V C	Default	circle (25um)	none	none		None		
fetal6 D	Default	circle (25um)	none	none		None		
/ia5 N	Vone	none	none	none		None		
fetal5	lone	none	none	none		None	~	
Default mapping	Anti pa	d None	Thermal pad Shape: ∱	Ione 💌	Con	ition data has changed nection point ction: None		Top view



#### Create Solderball Reference for Bottom Via 2

In the In Apply Padstack definition changes window ...

- Select Create new definition
- Select All vias and pins in the active design that use this definition
- Click the **OK** button

Properties		Ψ×	
Name	Value	Unit	
Туре	Via		
LockPosition			
Name	via_2029		
Net			
Padstack Definition	Solder_Template2		
Padstack Usage			
Start Layer	AP		
Stop Layer	Metal5		
Solder Ball Layer	BRD		
Backdrill Top			
Backdrill Bottom			
OverrideHoleDiameter			
HoleDiameter	15	um	
Location	0.2085652068949	mm	
Angle	0	deg	

Apply Padstack Definition Changes	$\times$
Padstack definition 'Solder_Template' used by 'via_2029'	
<ul> <li>Edit current definition</li> <li>Change all vias and pins that use this</li> <li>Create new definition</li> <li>Change</li> </ul>	
<ul> <li>Only this via or pin</li> <li>All vias and pins in the active design that use this d</li> </ul>	efinition
ОК Са	ncel

Notice how there is now a new *Padstack Definition* Solder\_Template<sup>2</sup>.



# Select Edges for First Gap Port at Top

- In the *Ribbon*, with the Layout tab selected, click on *Select Edges* (or just click the *E* key)
- Select the two edges on either side of the gap. *This gap port will be horizontally oriented.*





Select Edges

mode cursor

## Create First Gap Port - OnChip\_OctSpiralL1.aedt





## Create Second Gap Port at Bottom

• From the top of the GUI, select *Draw > Port > Create*.







## Both Ports Complete - OnChip\_OctSpiralL2.aedt







## Metal 5 and Metal 6 Final Via Stop Layer Check





## DC Continuity Check - Select Physically Connected

Layout HFSS 3D Layout Tools Window Help List... Fit All Dunite Ø Layers... € Ţ the Coloradoral 💟 Subtrac List... Nets 🗊 Intersed Push Down Select Physically Connected **~** Pop Up Select Net Connected Place Design... **Toggle Net Highlight** Snap 3D Select All Net Violations Connect Pins... Select First Violation Cutout Show Selected Nets Only Group into Subdesign Show All Nets Import 3D CAD... Export... > Cross-Probe Schematic Ctrl+K Settings... 2 Grid settings... Draw HFSS Air Box Draw HFSS Ports **-**ViaStyles... PinStyles... Line Styles... Text Styles... Export to Slwave with ALinks

A good way to check or troubleshoot a design is checking the DC continuity through *Layout > Nets > Select Physically Connected*.



In these pictures we're checking that the vias are all connected in a DC path from port to port through layer **BRD**. The spiral is not part of this.



## View HFSS Extents - OnChip\_OctSpiralL2.aedt

In the *Ribbon*, with the Layout tab selected, on the far right, click on the *Extents* icon and select *Show* (if the *Extents* airbox is not already showing).









In the *Ribbon*, with the Layout tab selected, on the far right, click on the *Extents* icon and select *Edit* to bring up the *Set HFSS Model Extents* dialog window.



- Set ...
  - 1. Dielectric section:
    - Horizontal Padding: 0.1
  - 2. Airbox section
    - Horizontal Padding: 0
    - Vertical Padding: 0.3
    - Sync: 🗹
  - 3. Click the **OK** button to close the window.

Set HFSS Model Extents
HFSS Bounds Defaults
✓ Open Region
Radiation
operating Frequency. SGHZ
Radiation Factor:
Lo H
Extents
Turne: Bounding Box
Polygon:
Dielectric
Horizontal Padding: 0.1
Users similians en distantia lavara
Honor primitives on dielectric layers
Airbox
Truncate model at ground layers
Horizontal Padding: 0
Vertical
Positive Padding: 0.3 🔽 Sync
Negative Dadalizaria
Negative Padding: 0.3



## View Final Edited HFSS Extents

Airbox	
Truncate model at ground layers	
Horizontal Padding: 0	
Vertical	
Positive Padding: 0.3	Sync
Negative Padding: 0.3	

The *Sync* checkbox synchronizes the *Airbox Negative Padding* with the *Positive Padding*.



#### Create HFSS Solution Setup

- In the *Project Manager*, right-click on *Analysis* and select *Add HFSS Solution Setup* 1. Click the *General* tab:
  - Setup Name: HFSS Setup1
  - Solution Frequency: 5 GHz
  - Maximum Number of Passes: 20
  - Maximum Delta S: 0.02
  - Save fields
  - 2. Click the **OK** button The frequency sweep setup dialog will automatically appear
- In the *Edit Frequency Sweep* tab dialog box
   *Name*: Sweep 1
  - **1.** Name: Sweep 1
  - 2. ☑ Use Q3D to solve DC point
  - 3. Sweep Type: Interpolating
  - 4. Specify *Frequency Sweeps* section
    - Distribution: Linear Step
    - Start: 0 GHz
    - Stop: 5 GHz
    - *Step*: 0.1 GHz
  - 5. Press the **OK** button

HFSS Setup 1		-
General Options Ad	vanced Advanced Meshing Solver DC R Defaults	
Setup Name:	HFSS Setup 1	
	Enabled	
Adaptive Solutions		
Solution Frequency	Single O Multi-Frequencies O Broadband	
Frequency	5 GHz 💌	
Maximum Numbe	of Passes: 20	
Maximum Delta S	0.02	
	Edit Frequency Sweep	
Fields	Edit Frequency Sweep Interpolation	
Save fields	Sweep Name: Sweep 1	✓ Enabled
🔲 Save radia	Sweep Type: Interpolating	Use Q3D to solve DC point
	Frequency Sweeps [51 points defined]	
	Distribution Start End	
	1 Linear Sten 0CHz 5CHz	Sten size 0.1CHz



#### Output Variables for Inductance and Quality Factor Plots

Equations for the inductance of a spiral inductor, often expressed in terms of Y-parameters, depend upon the configuration of the spiral inductor ports. In order to facilitate the ability to plot many calculated quantities, like inductance and quality factor Q, we can define equations as *Output Variables* for HFSS to plot in *Reports*.

 $L = \frac{im\left(\frac{1}{Y_{11}}\right)}{2\pi f} \qquad \qquad Q = abs\left(\frac{im\left(\frac{1}{Y_{11}}\right)}{re\left(\frac{1}{Y_{11}}\right)}\right)$ 

• To access the *Output Variables* definitions, in the *Ribbon*, with the Results tab selected, click on the *Output Variables* icon.

(Or ... alternatively ... from the top menu select item HFSS 3D Layout > Results > Output Variables...)

Image: CutImage: Cut<	Open Output	R Dele	te All Reports	Standard
	Report Variables	Mod	ify Report	Report T
Deskton View Lavout	Simulation	Poculte	Automation	

output rundbied		
Validate outp	out variables for selected context	
	Name	Expression
		Add

*Expression* is the equation of interest and *Name* is what appears in the *Report* window for plotting.



#### Creating an Output Variable for Inductance - Ind\_Spiral

- Bring up the *Output Variables* window and set:
  - Name box: Enter Ind\_SpiralA
  - Expression box, type 1e9\*im((1/
    - Category: Select Y Parameter from the drop-down box
    - Quantity: Y(Port1, Port1)
    - Click the Insert into Expression button
  - In the Expression box, type: ))/(2\*pi\*F)
  - Final Expression:

1e9\*im((1/Y(Port1, Port1)))/(2\*pi\*F)

- Click the **Add** button

1e9: Inductance will be reported will be in nH'pi' is a constant variable which is pre-defined'F' is an intrinsic variable defined for the Frequency



Output Variables	
Output Variables	ontext
Name	Expression
Name: Ind_Spiral	Add
Expression: 1e9*im((1/Y(Port1,Port1)))/(2	*pi*F)



### Finished Output Variable for Inductance - Ind\_Spiral

Ind\_Spiral will be a signal available to the *Results* to plot in *Reports*.

I _	$im\left(\frac{1}{Y_{11}}\right)$
<b>L</b> –	$2\pi f$

Name		Expre		
1 Ind_Spiral	1e9*im((1/	Y(Port1,Port1)))/(2*	i*F)	
Name:			Add	Update Delete
Context Report Standard Type: Solution: HFSS Setup 1 : Sweep 1	•	Quantities Category: Y Quantity: Y(Port1,Port1)	arameter	Function:
Context Report Standard Type: Solution: HFSS Setup 1 : Sweep 1 Domain: Sweep	- - -	Quantities Category: Y Quantity: Y(Port1,Port1) Y(Port2,Port1) Y(Port1,Port2) Y(Port2,Port2)	<sup>2</sup> arameter	Function: <pre> acos acosh ang_deg ang_deg ang_rad arg asin asinh </pre>



#### Creating an Output Variable for Quality Factor - Q\_Spiral

- Bring up the *Output Variables* window and set:
  - Name box: Enter Q\_SpiralA
  - Expression box, type abs(im((1/
    - Category: Select Y Parameter from the dropdown box
    - Quantity: Y(Port1, Port1)
    - Click the *Insert into Expression* button
  - *Expression* box, type: ))/re((1/
    - Category: Select Y Parameter from the dropdown box
    - Quantity: Y(Port1, Port1)
    - Click the Insert into Expression button
  - Expression box, type: ))
  - Final Expression:

#### abs(im((1/Y(Port1,Port1)))/re((1/Y(Port1,Port1))))

Click the **Add** button

	$\left\langle re\left(\frac{-}{Y_{11}}\right)\right\rangle$
output Variables	
Output Variables	ontext
Name	Expression
1 Ind_Spiral	1e9*im((1/Y(Port1,Port1)))/(2*pi*F)
Name: Q_Spiral	Add
Expression: abs(im((1/Y(Port1,Port1)))/re(	(1/Y(Port1,Port1))))

 $\boldsymbol{Q} = \boldsymbol{abs}\left(\frac{\boldsymbol{im}\left(\frac{1}{\boldsymbol{Y}_{11}}\right)}{\boldsymbol{im}\left(\frac{1}{\boldsymbol{im}}\right)}\right)$ 

**1e9**: Inductance will be reported will be in **nH** 

- **'pi'** is a constant variable which is pre-defined
- **'F'** is an intrinsic variable defined for the **Frequency**

## Finished Output Variable for Q - Q\_Spiral - OnChip\_OctSpiralL2.aedt

**Q\_Spiral** will be a signal available to the *Results* to plot in *Reports*.



💵 Output Variables	×
Output Variables	ontext
A Name	Expression
1 Ind_Spiral	1e9*im((1/Y(Port1,Port1)))/(2*pi*F)
2 Q_Spiral	abs(im((1/Y(Port1,Port1)))/re((1/Y(Port1,Port1))))
Name:	Add Update Delete
Expression:	
Context	Quantities
Report Standard	Category: If Parameter
Solution: HFSS Setup 1 : Sweep 1	V(Port1,Port1) <pre><pre></pre></pre>
Domain: Sweep	Y(Port2,Port1)     acos       Y(Port1,Port2)     ang_deg       Y(Port2,Port2)     ang_deg_val       ang_rad     arg       asin     asin       asin     asin
- Function	Insert Into Expression
abs Insert into Expre	Import Export Done



#### Modify Solution Setup to Add Output Variable Mesh Convergence

HFSS	Setup 1				×							
Gene	eral Options A	Advanced A	Advanced Meshin	g Solver DC R	Defaults							
5	Setup Name:	HFS	S Setup 1									
	Enabled											
Ad	aptive Solutions											
So	olution Frequenc	y: O	Single 🕡 Mu	lti-Frequencies	C Broadband							
	Frequency	Units	Max Delta S	Output Var	Add							
	2.5	GHz	0.02	Add								
	5	GHz	0.02	Add								
	10	GHz	0.02	Add	Remove							
Fie	Maximum Numb	er of Passes	20									
	Save fields											
	🔲 Save rad	liated fields (	only									
			Use Defaults	3								
				HPC and Analy	sis Options							
				ОК	Cancel							

- Modify existing *HFSS Solution Setup*:
  - In the *Project Manager*, under *Analysis*, double-click on the *HFSS Setup 1* to bring up the *Solution Setup* tab dialog box.
  - Under *General* tab, check *Multi-Frequencies* radio button
    - On the 5 GHz line, below the Output Var column, click the Add... button
    - Include **☑** for all the *Output Variables*
    - Max. Delta = 0.05 for Inductance and 0.05 for Quality factor.
  - Click the **OK** button twice in a row to close both windows.

dvanced Mesh Convergence Criteria at 5.0000GHz Output Variable Include Max Delta									dvanced Mesh Convergence							
Criteria at 5.0000GHz Output Variable Include Max Delta Ind_Spiral																
Output Variable	Include	Max Delt	ta													
Ind_Spiral	~	0.05														
Q_Spiral	~	0.05														
	eria at 5.0000GHz Output Variable Ind_Spiral Q_Spiral	eria at 5.0000GHz Output Variable Include Ind_Spiral Q_Spiral	eria at 5.0000GHz Output Variable Include Max Delt Ind_Spiral Q_Spiral O.05													



## HPC Setup - OnChip\_OctSpiralL3.aedt

- Save Project to OnChip\_OctSpiralL3.aedt ٠
- In the *Ribbon*, with the Simulation tab selected, click ٠ on the icon *HPC Options* to bring up the *HPC and* Analysis Options tab dialog box.
  - Design Type: HFSS 3D Layout Design
  - Select the Active Configuration: Local
  - In the middle of the window, click on the *Edit* button to open the Analysis Configuration window.
- In the *Analysis Configuration* window ... •
  - Check the option for *Use Automatic Settings*
  - Click the *Machines* tab
    - Name: localhost •
    - *Cores*: 4 (or 7 if 8 cores are available)
    - **RAM Limit** (%): **90** •
    - Click the **OK** button to close **Analysis** • Configuration
  - Click the **OK** button to close **HPC and Analysis Options**

HPC and	d Analysis Options						
Configuratio	ons Options						
Design Ty	pe: 🙋 HFSS 3D Layou	ut Design	•				
Available	Configurations:			Configuratio	n Details:		
Active YES	Name Local	Total Tasks Auto	Make Active	Configuratio	n Name:		
			Add Edit	Machine Lis Iocalhost(A Job Distribu	uto):7:90%		
			Analysis Configuratio	'n			
		Conf	iguration name: Loca				
		I ∪ Nui Ma	The I Jse Automatic Settings m variations to distribut uchines Options	e: 1	active job configurations	5	
			Machines for Distribute	d Analysis			
			Total Enabled Cores:	7	DAMLimit (%)	Enabled	
			localhost	7	90		
			Machine Details:				



#### Validate and Simulate OnChip\_OctSpiralL3.aedt

- Save the project **OnChip\_OctSpiralL3.aedt**.
- In the *Ribbon*, with the **Simulation** tab selected, click on the green check mark to validate the simulation.
- Click on *Analyze* to start the simulation.
- In the *Project Manager*, even while the simulation is running, under *Analysis*, right-click on the HFSS Solution Setup and select *Profile*
  - To view the *Profile*, click the *Profile* Tab
  - To view the *Convergenc*e, click the *Convergence* Tab
  - To view the *Matrix Data*, click the *Matrix Data* Tab
- Press the *Close* button when you are finished.

Adaptive passes are performed till both Mag. Delta S < 0.02 and Delta for Inductance < 0.05 and Delta for Q < 0.1



Solutions: OnChip_OctSpiralL3 - Spiral	_Ind			_
Simulation: HFSS Setup 1	•			
Design Variation:				
Profile Convergence Matrix Data				
- Number of Passes	Pass Number	Solved Elements	Max Mag. Delta S	Delta Output Var
Completed 6	1	4354	1	N/A
Maximum 20	2	5636	0.84091	Ind_Spiral=2.342; Q_Spiral=0.8785
Minimum 1	3	7216	0.264	Ind_Spiral=0.536; Q_Spiral=0.1822
-Max Mag. Delta S	4	9229	0.069459	Ind_Spiral=0.1554; Q_Spiral=0.07323
Target 0.02	5	11750	0.029702	Ind_Spiral=0.1258; Q_Spiral=0.107
Current 0.010834	6	14979	0.010834	Ind_Spiral=0.08755; Q_Spiral=0.00139
View:  Table Plot				



## **OnChip\_OctSpiralL3.aedt** Simulation Results - Inductance Report

- In the *Ribbon*, with the **Results** tab selected, click *Standard Report* and select *2D*.
  - Solution: *HFSS Setup1: Sweep 1*
  - Domain: Sweep
    - Category: Output Variables
    - Quantity: Ind\_Spiral
    - Function: <none>
    - Click *New Report* button
  - Click the *Close* button

es		Standard Sol Report ▼ D	ution Ne Data Data	twork Explorer
Report: OnChip_OctSpiralL3 - Spiral_I Context Solution: HFSS Setup 1 : Sweep : Domain: Sweep	nd - New Report - New Trace(s)          Trace       Families       Families Display         Primary Sweep:       F       All         X:       V       Default		Stacked	Polar
	Y: Ind_Spiral Category: Quantity:	Smith Chart Function:	3D	3D Polar
Update Report       Image: Constraint of the second se	Variables       Ind_Spiral         Output Variables       Q_Spiral         S Parameter       Q_Spiral         Y Parameter       Z Parameter         Group Delay       V         Return Loss       V	<pre><none> abs acos acosh ang_deg ang_deg </none></pre>		
Output Variables Options	New Report         Apply Trace         Add Trace		Close	



2

## S-Parameters Intuitive Trouble Shooting Check

Before looking at the main results for this workshop, the inductance and quality factor, we can do a quick intuitive check using S-parameters. At low frequencies we expect large transmission and small reflection.





Post

Processing

#### Viewing OnChip\_OctSpiralL3.aedt Simulation Results: Inductance

- In the *Project Manager,* under *Results*, right-click on the report and select *Rename*.
- Change the name of the report to Spiral Inductance.





Post Processing

## **OnChip\_OctSpiralL3.aedt** Simulation Results - Quality Factor

- In the *Ribbon*, with the **Results** tab selected, click *Standard Report* and select *2D*.
  - Solution: *HFSS Setup1: Sweep 1*
  - Domain: Sweep
    - Category: Output Variables
    - Quantity: Q\_Spiral
    - Function: <none>
    - Click *New Report* button
  - Click the *Close* button

les		Standard Sol Report ▼ D	ution Network Data Data E	vork xplorer
Report: OnChip_OctSpiralL3 - Spiral_I Context Solution: HFSS Setup 1 : Sweep :	nd - Output Variables Plot 2 - Q_Spiral Trace Families Families Display Primary Sweep: F  All	2D	CAAJIM CAAJIM MMMMM Stacked	Polar
Domain: Sweep 💌	X: Default F Y: Q_Spiral	Smith Chart	3D	3D Polar
Update Report Real time	Category: Quantity:  Variables Variables S Parameter Y Parameter Z Parameter Group Delay Return Loss Variables Varia	Function: abs acos acosh ang_deg ang_deg val < 2		
Output Variables Options	New Report Apply Trace Add Trace		Close	



2

### Viewing OnChip\_OctSpiralL3.aedt Quality Factor Report

- In the *Project Manager,* under *Results*, right-click on the report and select *Rename*.
- Change the name of the report to Spiral Q



Post Processing

#### Solve Options: *Solve Inside* or DC thickness

The default setup for HFSS assumes current flow only on surface of metals. For on-chip applications, circuit dimensions are very small (order of  $\mu$ m). In many cases, for an accurate answer, the skin effect must be modeled and simulated.

HFSS 3D Layout offers two ways to capture skin effect:

#### 1. Solve inside

Enables all the objects in the layer to have "Solve Inside" attribute set for HFSS solver

#### 2. DC thickness (By default)

Controls how DC thickness will be calculated for the conductor lumps on the layers.

 Verify that project
 OnChip\_OctSpiralL3.aedt got saved after making reports.

In HFSS online *Help*, search on skin effect or solve inside. There is one section, titled *Bulk Conductivity*, that talks about solve inside.



#### Copy Design to Spiral\_Ind\_SolveInside - Project OnChip\_SpiralL4

Make data copies of existing simulation data

- In the Project Manager, under Results, under each Report, rightclick on the data and select Copy Data.
- Right-click on the *Report* name and select *Paste*.
- Right-click on the new trace and rename it adding the word Data. This copied data won't change when we change the design and resimulate it.



- In the *Project Manager*, right-click on the design name Spiral\_Ind and select Copy.
- Right-click on the *Project* name *OnChip\_SpiralL3* and select *Paste*.
   A new design *Spiral\_Ind1* will be inserted in the project.
- Right-click on the new design *Spiral\_Ind1* and select *Rename*.
- Rename the new design to *Spiral\_Ind\_SolveInside*
- Save project to OnChip\_SpiralL4.aedt.







#### Set Solver Options to Solve Inside for Most Copper Layers

- Double-click on the new design Spiral\_Ind\_SolveInside
- Open the *Layer Stackup* window.
   Select the layers: *AP* through *Metal4* using the *Shift* key
  - 2. In the *Analysis* area ...
    - Check the box for *Solver*
    - Click the button *Solver...* 
      - Click the HFSS tab
      - Check the option for Solve inside
      - Click the **OK** button

#### 3. Click the *Apply and Close* button

Solver Options	$\times$
HFSS Planar EM Solve Options ✓ Solve inside DC Thickness: Effective	
OK Cancel	

Stackup I	ayer												
Display Stack Non-s All lay	up laye tackup ⁄ers	rs layers	S C	tackup – Lamin Inits: m	ate moi m	de	•						
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<b>ZZ</b>	~	~	<b>~</b>	~	<b>~</b>	~	ероху	dielectric	FR4_epoxy	200um			
			<b>~</b>	<b>~</b>		<b>~</b>	AP	signal	copper				
			<b>~</b>		<b>~</b>	<b>~</b>	RV	signal	copper				
			<b>~</b>			<b>~</b>	Metal6	signal	copper				
- 🗸			<b>~</b>		<b>~</b>	<b>~</b>	Via5	signal	copper				
			<b>~</b>			<b>~</b>	Metal5	signal	copper				
			~			~	Via4	signal	copper				
						Image: A start of the start	Metal4	signal	copper	1um			
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//nsys

## Analyze - Spiral\_Ind\_SolveInside

- Select the menu item *HFSS 3D Layout > Analyze*
- In the *Project Manager*, under *Results*, double-click on a plot name.
- Imported refers to the stored data. The red plots are from Solve Inside.

Simulating *Solve Inside* can take significantly more time than the previous simulation.

#### Inductance/Quality Factor plots using Solve Inside







