HFSS_3DLGS_2019R3_EN_ WS3.1_OctSpiral

HFSS 3D Layout Getting Started

WS3.1

On-Chip Octagonal Spiral Inductor

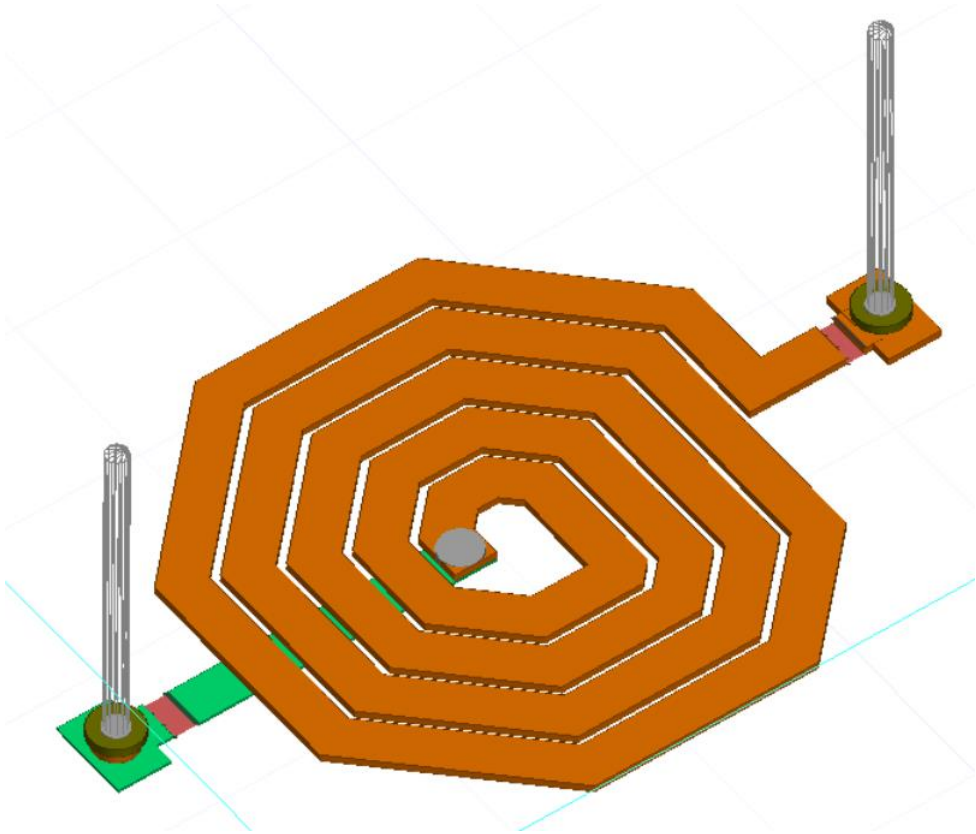
This workshop sets up and analyzes an octagonal spiral inductors using the ANSYS HFSS 3D Layout environment.

The following topics are covered in this example:

- Concept of equivalent inductance and return path
- Setting up vias
- Defining ports for simulation
- Defining output variables for L and Q-factor
- Analyzing the effect on inductance and quality factor using several Solver options
  (DC Thickness, Solve Inside)

Starting file for this workshop:

OnChip_OctSpiralL0.aedtz



Finished spiral inductor including via solderballs up to the BRD layer that is not shown here.

On Chip Spiral Inductor - Workshop Outline

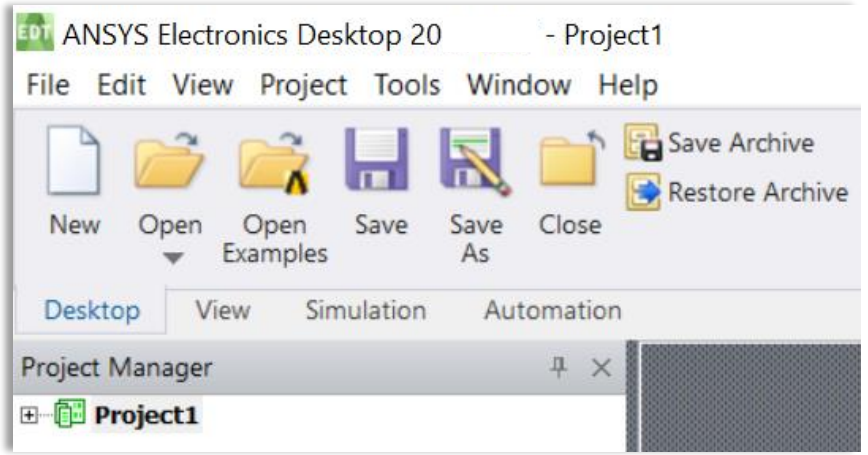
Outline of steps done in this workshop:

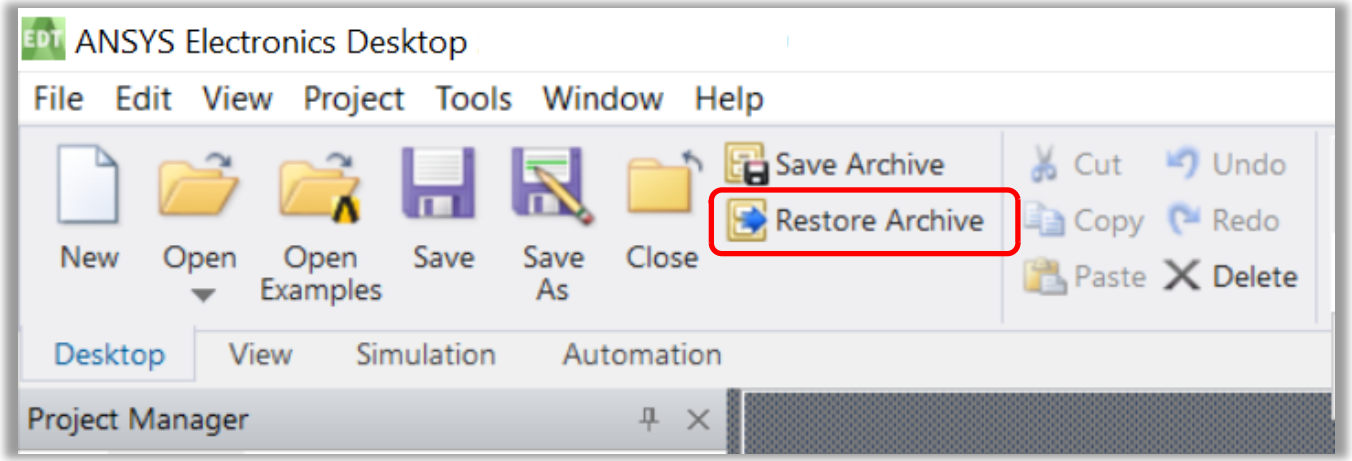
• Open archive file of octagonal spiral missing two vias	**OnChip_OctSpiralL0.aedtz**
• Add two vias including modifying the padstack definition.	**OnChip_OctSpiralL1.aedt**
• Add long vertical ground return current paths with the solderball files	
• Add two ports	**OnChip_OctSpiralL2.aedt**
• Adjust ***HFSS Extents*** to define the substrate and bounding box.	**OnChip_OctSpiralL2.aedt**
• Add HFSS ***Solution Setup*** for finite element method simulation	
• Add ***Output Variables*** for Inductance and Quality Factor	**OnChip_OctSpiralL2.aedt**
• Simulate and View Results	**OnChip_OctSpiralL3.aedt**
• ***Copy Data*** in Reports and then copy design for solve inside	**OnChip_OctSpiralL3.aedt**
• Set HFSS settings to solve inside for design **Spiral_Ind_SolveInside**	**OnChip_OctSpiralL4.aedt**
• Compare results from the two different simulations	**OnChip_OctSpiralL4.aedt**

Launching AEDT - HFSS 3D Layout - Restore Archive

Launch the ANSYS Electronics Desktop (AEDT) to access HFSS 3D Layout ***…***

- In Microsoft Windows, click the Microsoft Start button, select ***Programs > ANSYS EM Suite 20XXRY > ANSYS Electronics Desktop***
  A new ***Project1*** appears under the ***Project Manager***.
- In the ***Ribbon***, in the Desktop tab, select the icon for ***Restore Archive.***

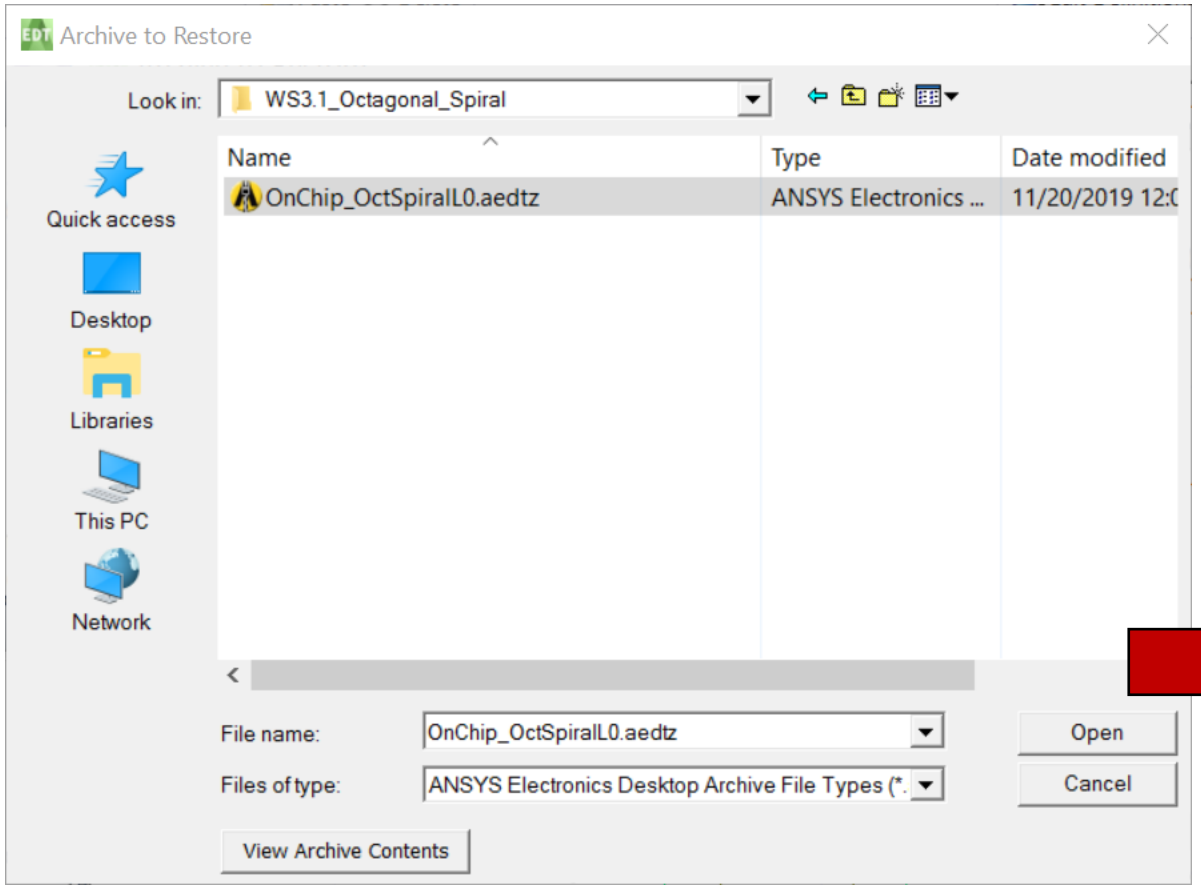


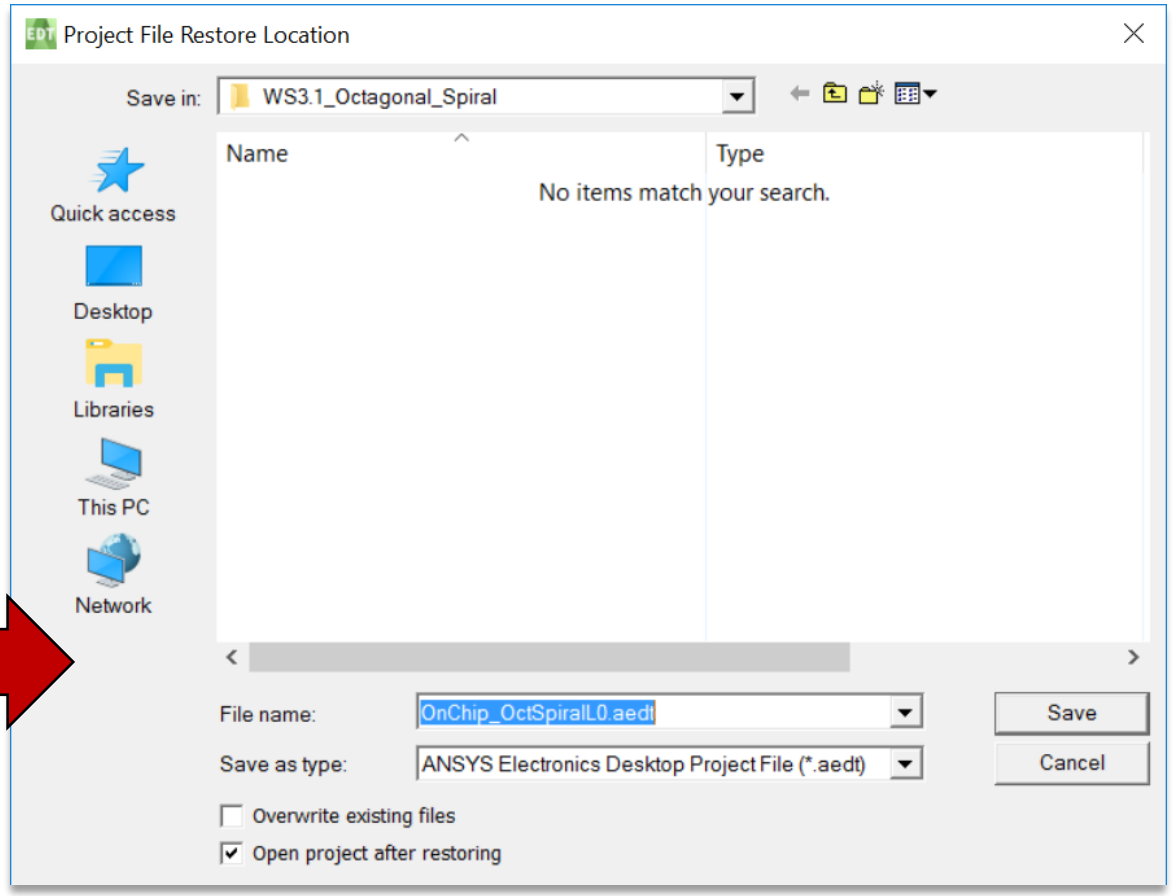


A windows browser will appear …

Restore Archive to OnChip_OctSpiralL0.aedt

- Browse to the training files and restore the file ***OnChip_OctSpiralL0.aedtz***
- Restore the file ***OnChip_OctSpiralL0.aedt*** to a working directory.



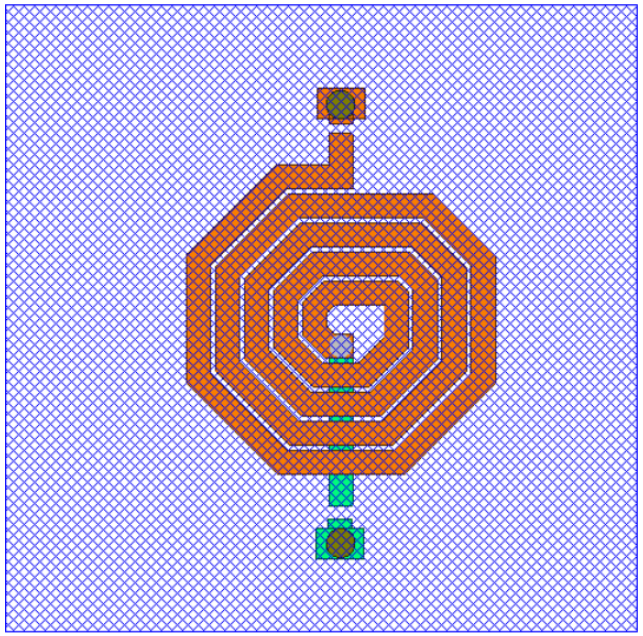


Spiral Inductor Layout

This initial spiral inductor has the dielectric padding and extents specified. The blue line around the spiral sets both the dielectric boundary and the airbox simulation space.

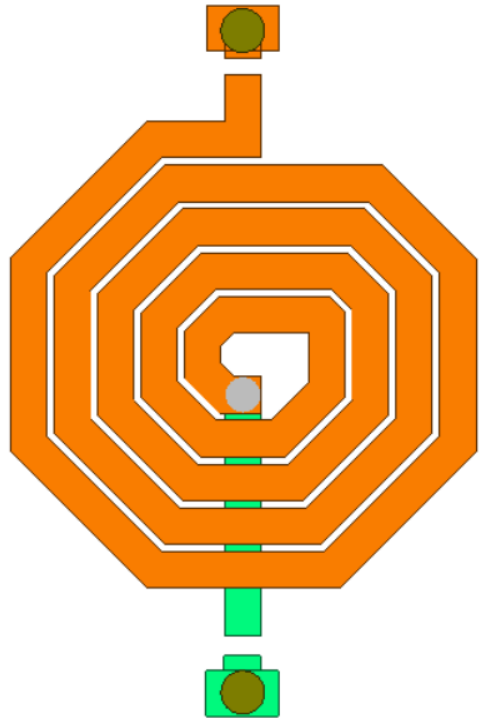
This initial spiral inductor is missing two vias, which will extend vertically up to a plane that completes the ground return current path.

This initial spiral inductor is missing two ports.



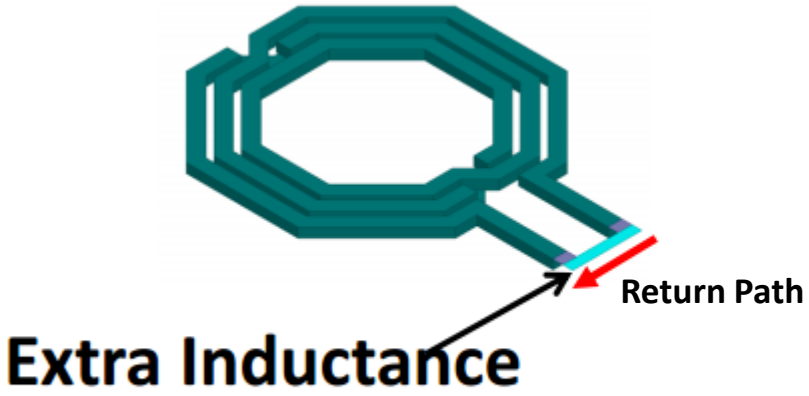
This ***Display Default*** view shows the rectangle, on the **BRD** level, to which the ***Extents*** conform.

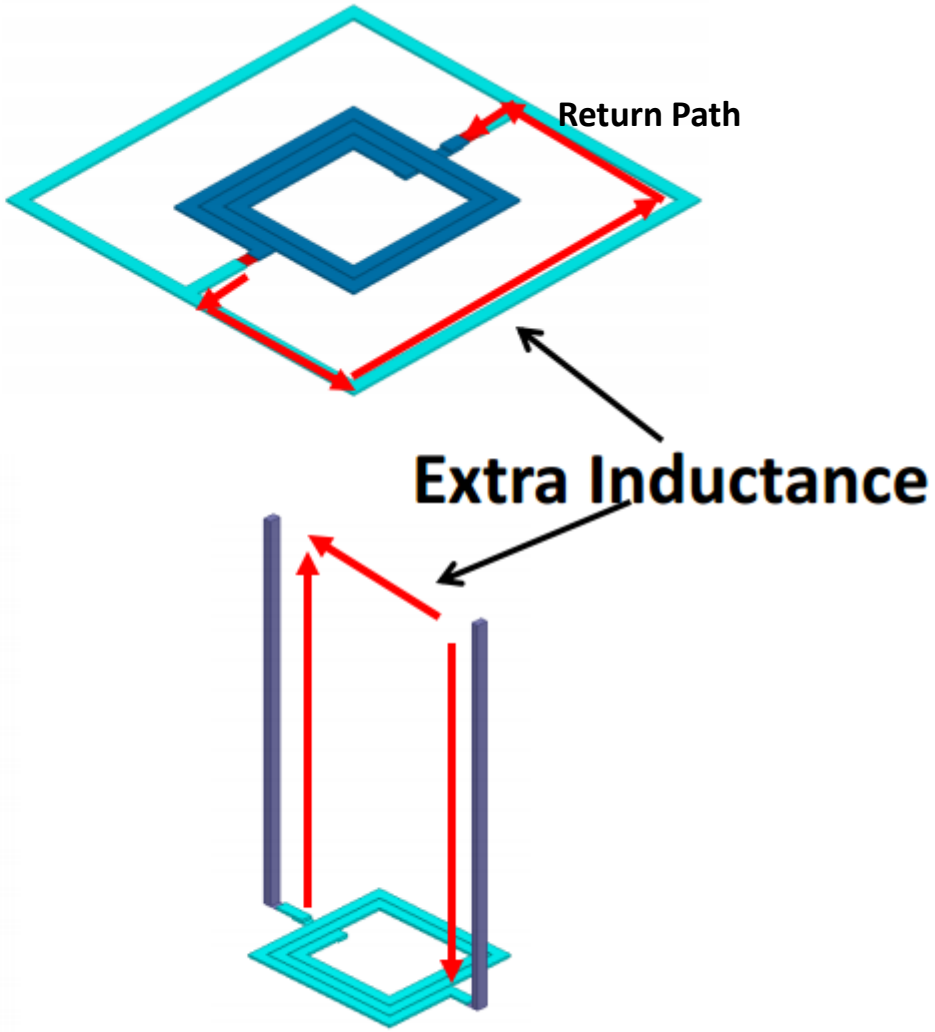
Airbox and Dielectric Padding boundary

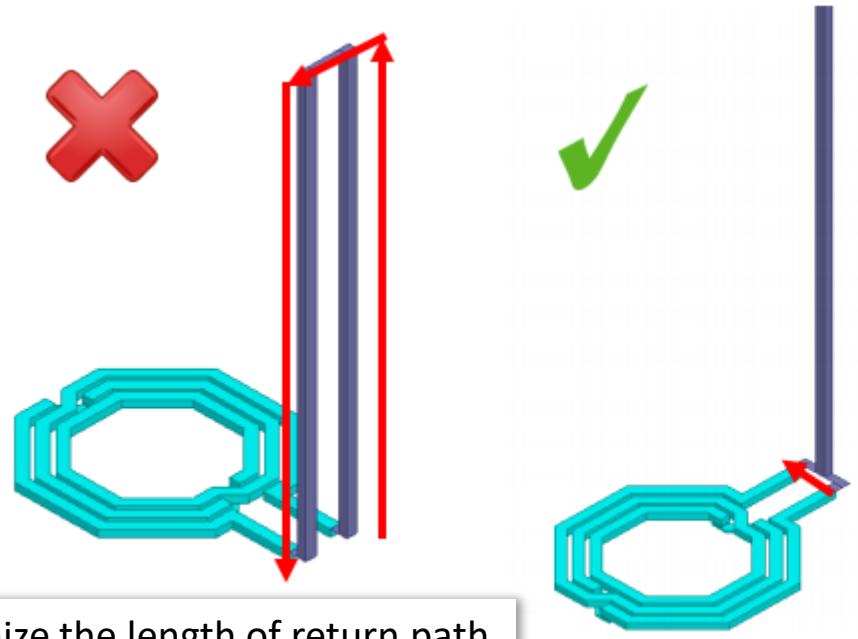


Airbox and Dielectric Padding boundary

Concept of Equivalent Inductance





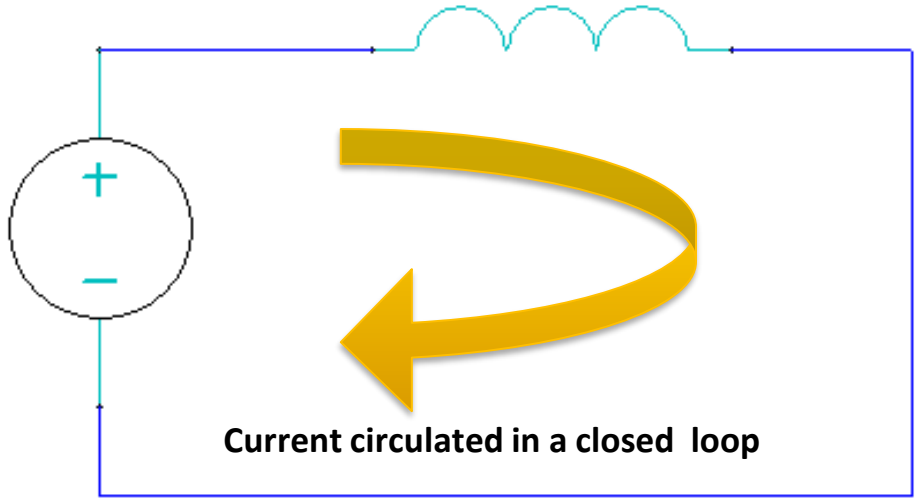


Minimize the length of return path

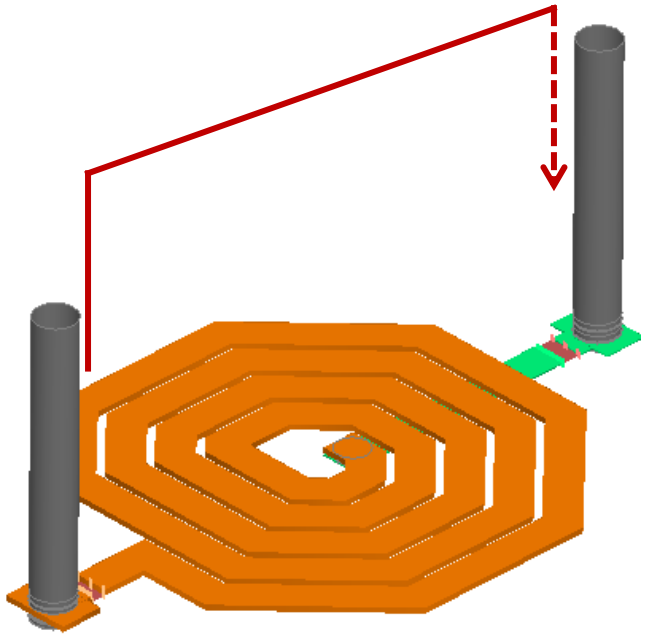
Concept of Equivalent Inductance in Our Spiral Inductor

HFSS calculates the equivalent Inductance of a net:

- Inductive and capacitive effects will be included.
- Loop inductance has more physical meaning than partial inductance.
- A close current loop must be formed in order to accurately simulate the loop inductance.

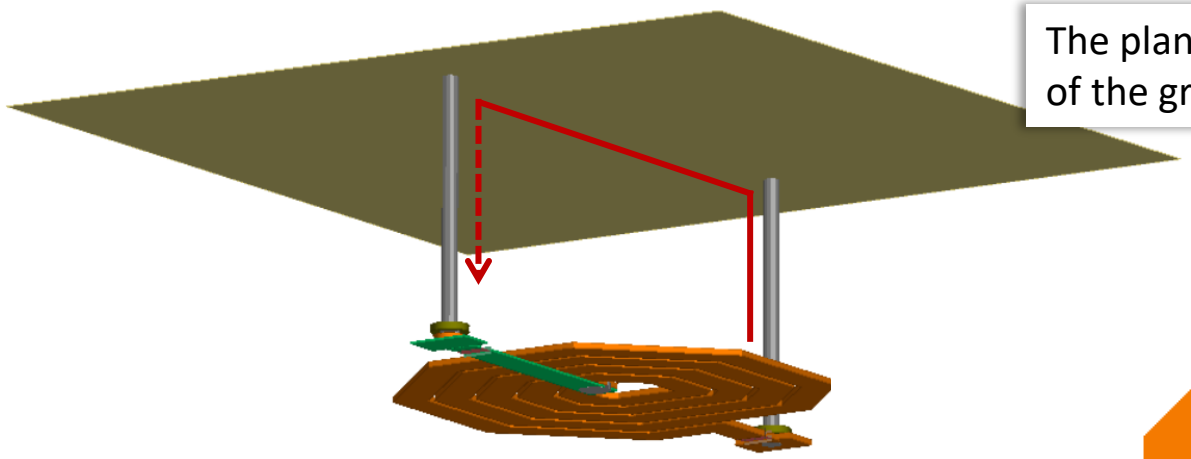


We'll construct very long(vertically) vias that create this return path through the BRD layer.

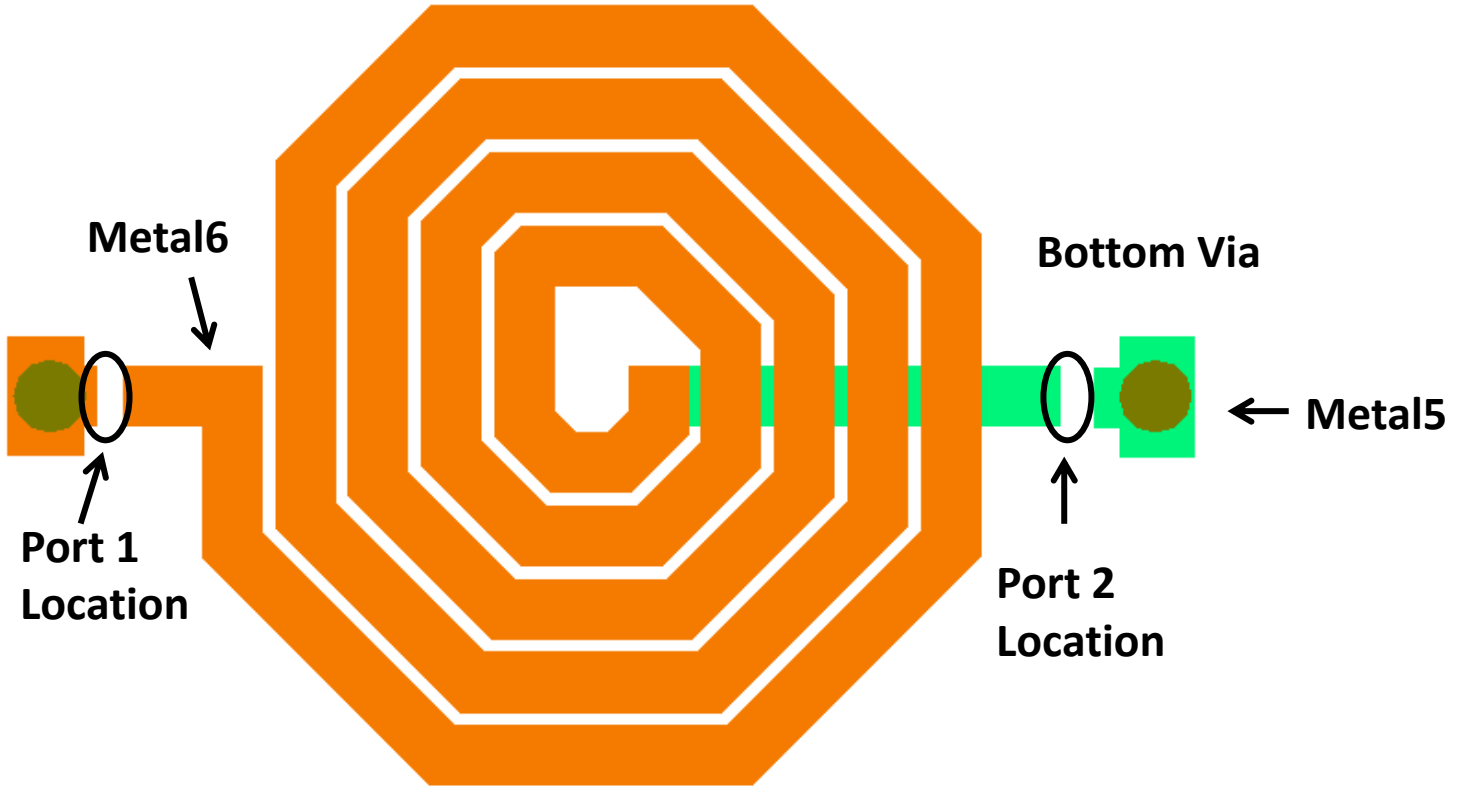


1. It is always recommended to include the real return path in a structure being simulated.
2. If it is not possible to add the real return path, we have to assume where the return path is going to be.

Spiral Geometry Overview



The plane on the BRD layer is part of the ground return current path.

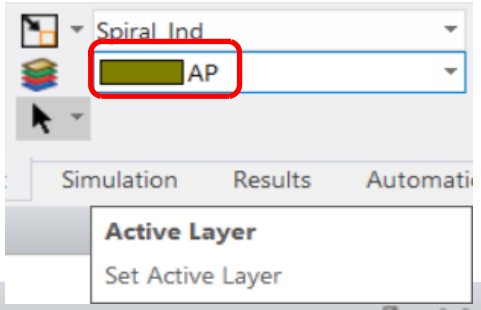


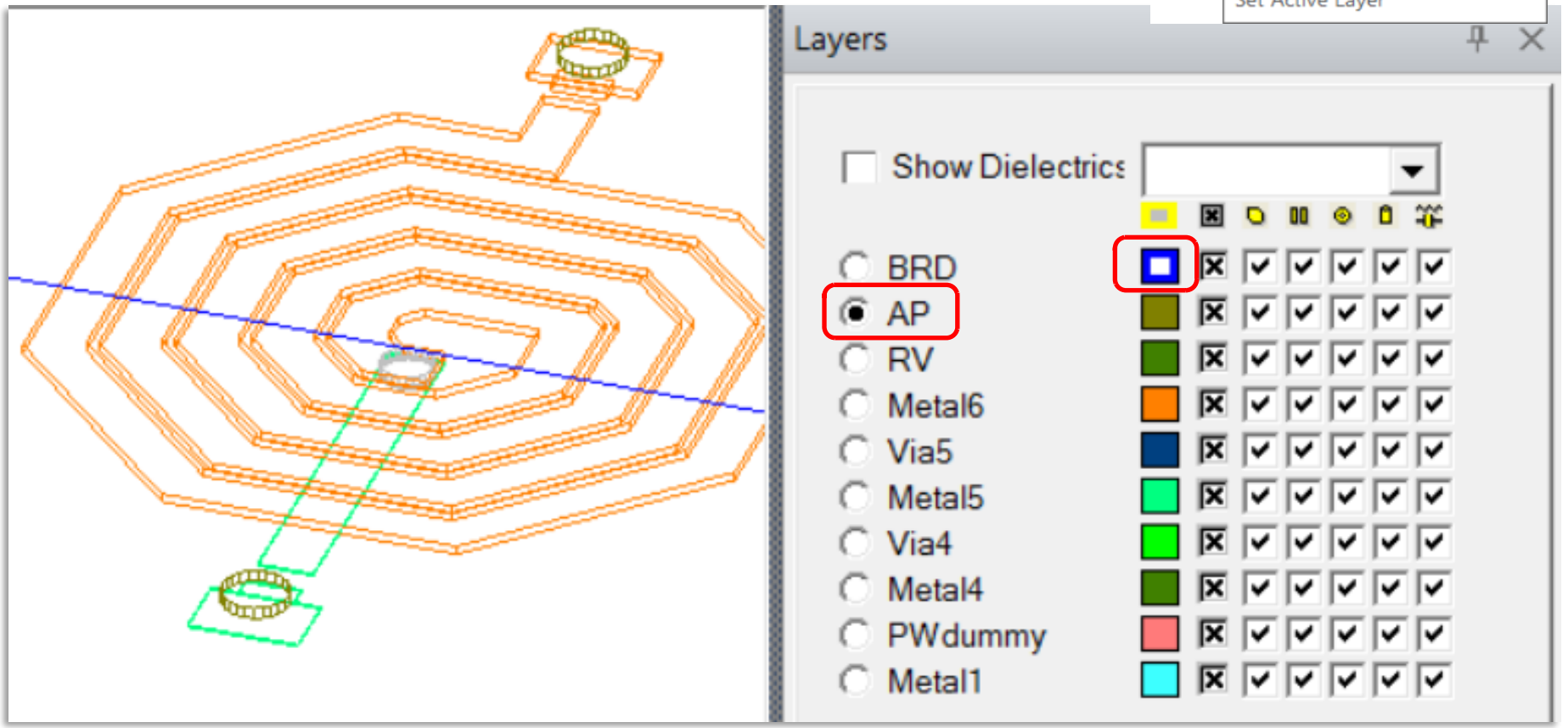
Setting up ports and adding additional perfect conductor leads will be discussed in next slides

Set Active Layer to AP - OnChip_OctSpiralL0.aedt

There are two ways to set the active drawing layer:

1. From the toolbar, locate the toolbar for the Active Layer, From the pull-down, select the layer ***AP***
2. In the Layout tab, use the ***Active Layer*** pull down



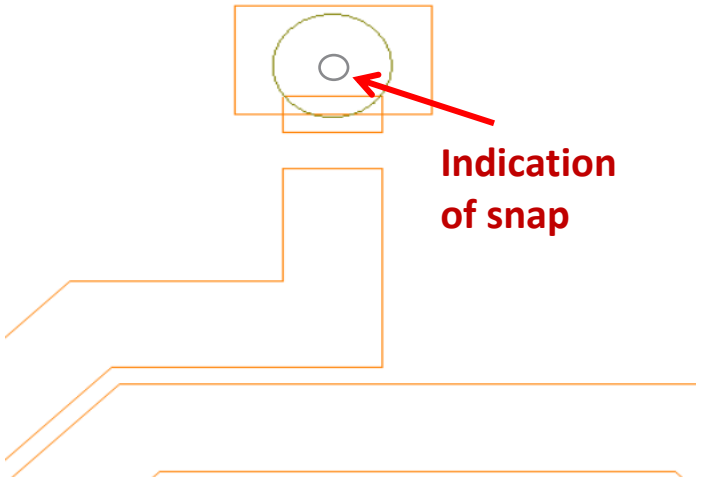


We're preparing to draw vias.

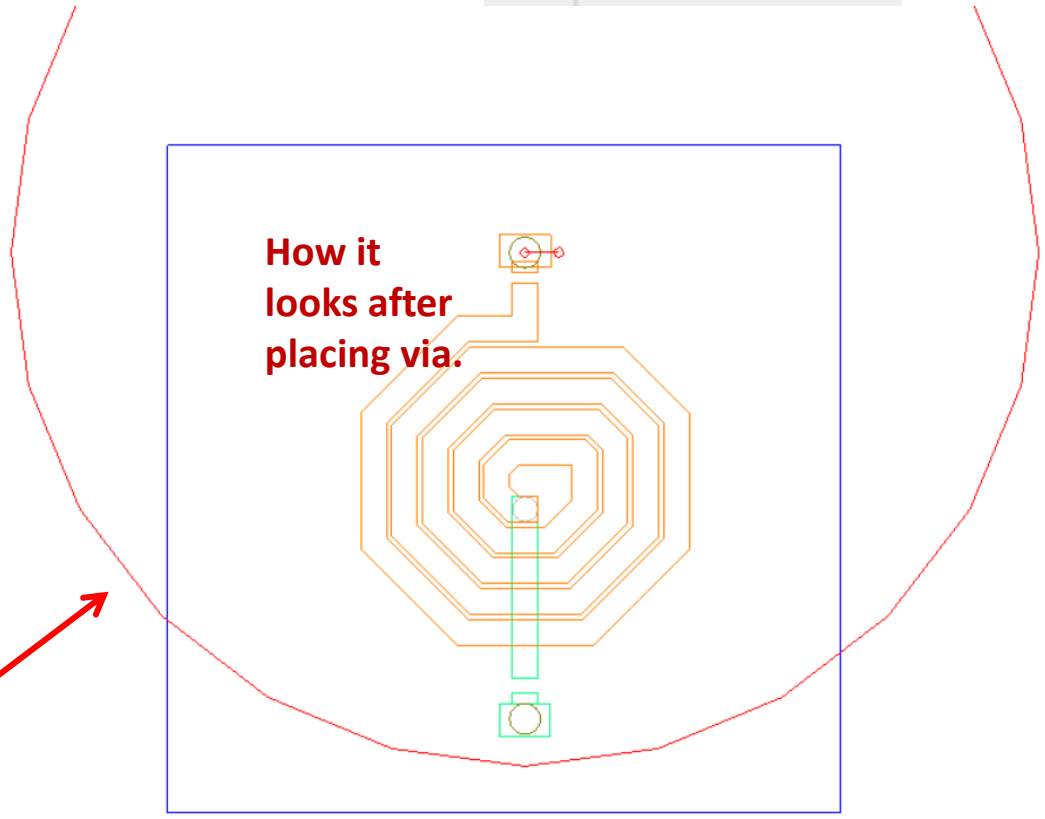
- Set ***Display*** to ***Sketch***.

Drawing a Via - Snap to Center of Circle

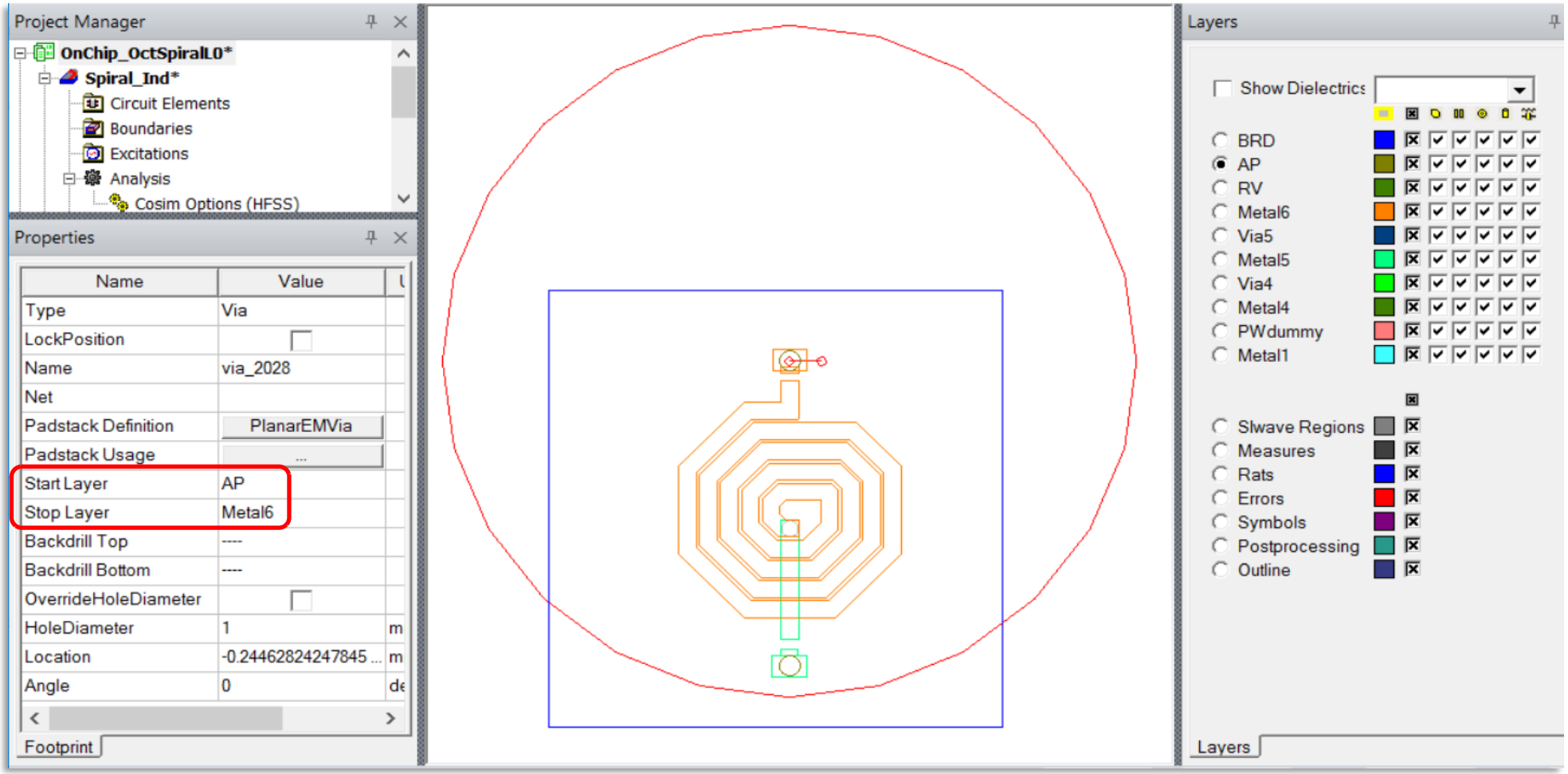
- Prepare to draw a Via:
  - Make sure that ***Snap object center*** is enabled. (Layout tab)
  - Shift to ***Top*** view
  - Set to ***Display Sketch***.
- Draw the via in the center of the circle:
  - Click on the icon for ***Draw Via***.
  - Move the cursor to the circle on the spiral.
  - Look for another circle to indicate snap to the circle center and click when the via is snapped.



Default size of via (diameter): 1mm



Modifying Via: Set Start and Stop Layers

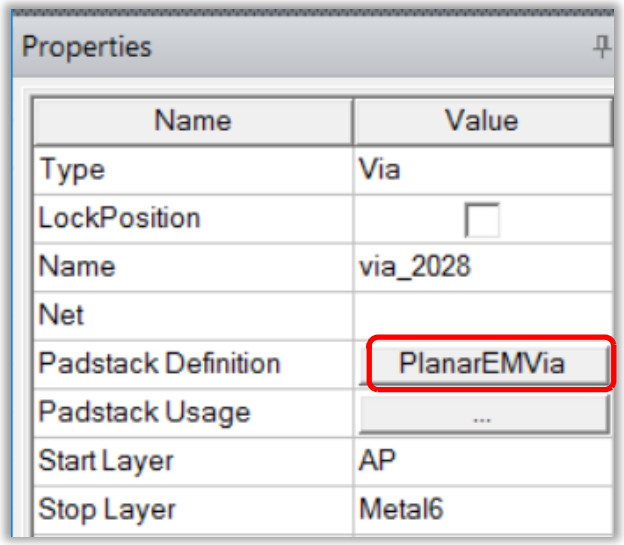


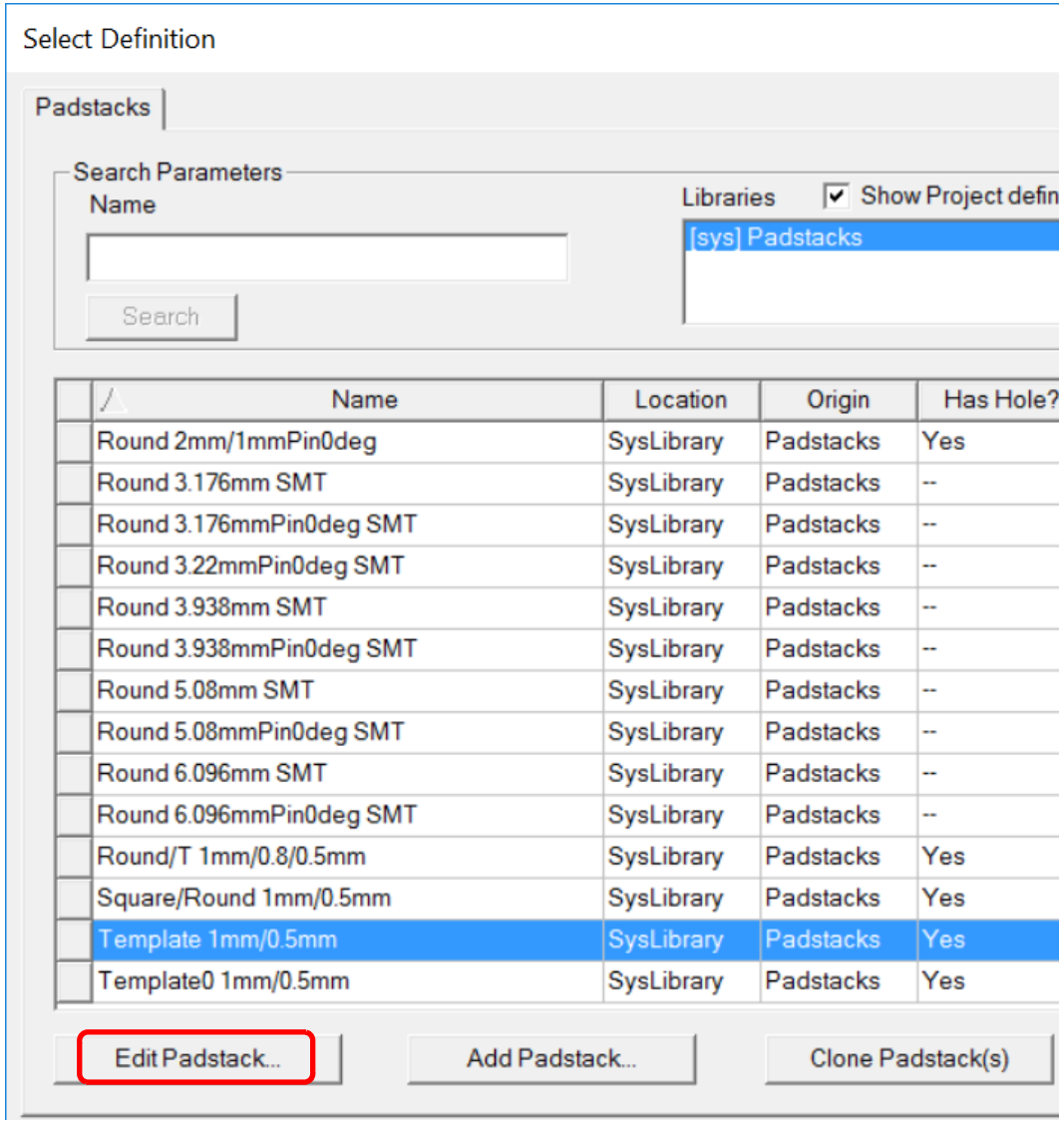
- Select the upper via.
- In ***Properties*** on the ***Padstack Definition*** line
  - Set Start Layer: **AP**
  - Set Stop Layer: **Metal6**

Modifying a Via: Modifying Padstack - Open Select Definition Window

In the ***Properties*** tab for the via …

- Click on the ***Value* PlanarEMVia**, to bring up the ***Select Definition*** window.
  - In the ***Select Definition*** window for the Padstacks
  - Scroll down to select ***Template 1mm/0.5mm*** and click ***Edit Padstack***..
  - In the ***Select Definition*** window click on the ***Edit Padstack*** … button to bring up the ***Edit Padstack Definition*** window.

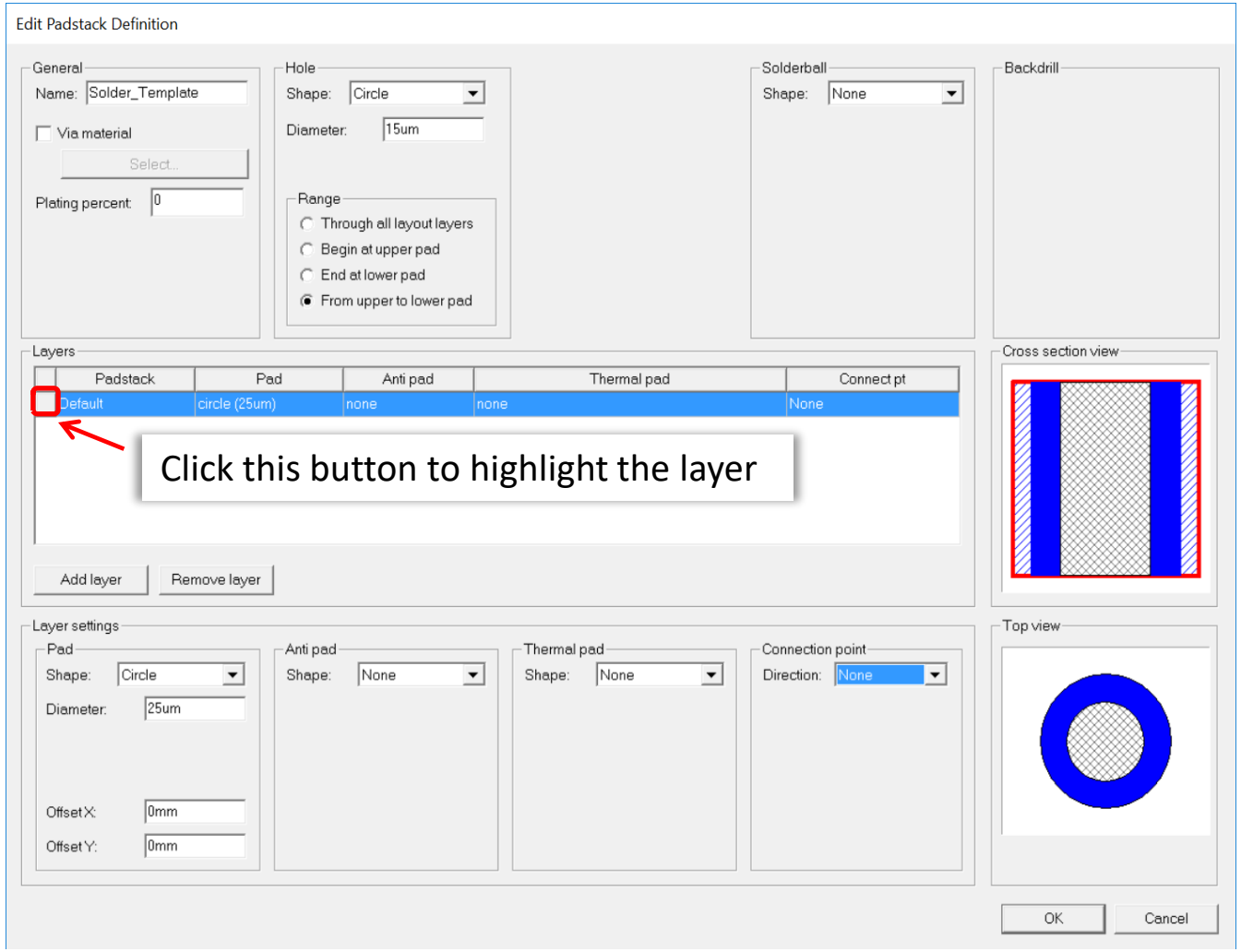




Edit Padstack Definition Window - OnChip_OctSpiralL0.aedt

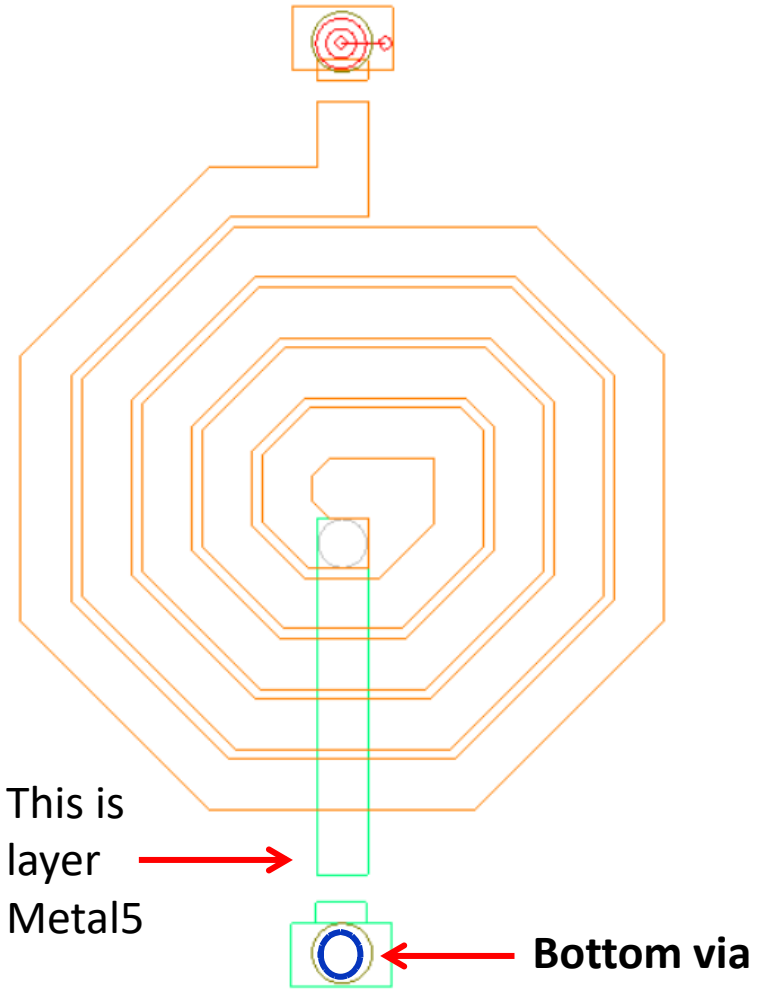
In the ***Edit Padstack Definition*** window

1. General settings:
   - ***Name***: **Solder_Template**
2. Hole settings:
   - ***Shape***: **Circle**
   - ***Diameter***: **15um**
3. ***Solderball***
   - ***Shape***: ***None***
4. In ***Layers*** section, click on the button to highlight the layer
   - ***Pad*** settings:
     - ***Shape***: ***Circle***
     - ***Diameter***: **25um**
   - ***Anti pad*** settings:
     - ***Shape***: ***None***
   - ***Thermal pad*** settings:
     - ***Shape***: ***None***
   - ***Connection point*** settings:
     - Direction: ***None***
5. Click the ***OK*** button to close this window and then to close the ***Select Definition*** window.



Copying the Top Via to the Bottom - OnChip_OctSpiralL1.aedt

In the layout, with the top via selected:
- Select the menu item ***Edit > Copy***
- Select the menu item ***Edit > Paste***
- Move the cursor to the lower circle and click after it snaps to the object.



Properties

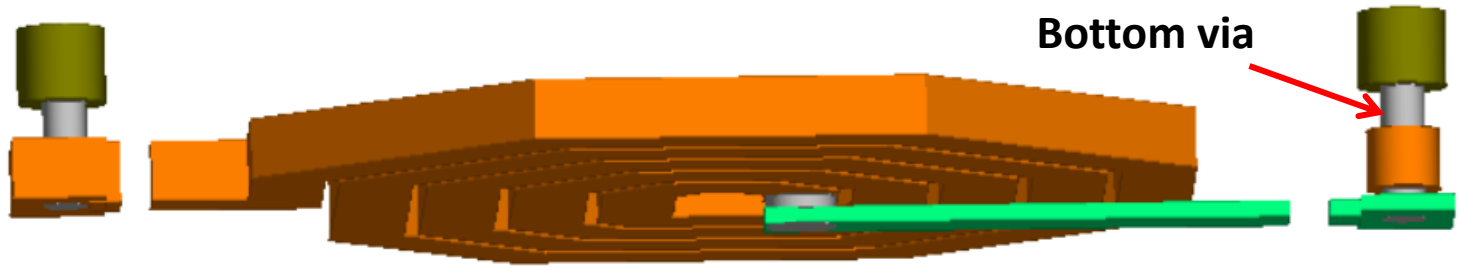
Name	Value
Type	Via
LockPosition	☐
Name	via_2029
Net	
Padstack Definition	Solder_Template
Padstack Usage	...
Start Layer	AP
Stop Layer	Metal5
Backdrill Top	----
Backdrill Bottom	----
OverrideHoleDiam...	☐
HoleDiameter	15

- In the ***Properties*** window for the bottom via change:
  1. Start Layer: ***AP***
  2. Stop Layer: ***Metal5***

- Save the project as **OnChip_SpiralL1.aedt**.

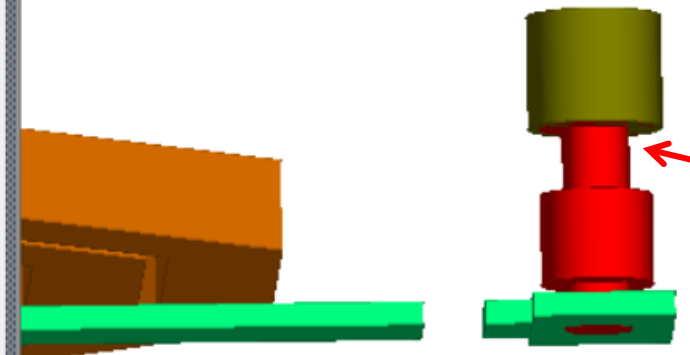
View Both Vias with Z-Stretch - OnChip_OctSpiralL1.aedt

In the layout, the vertical dimension can be stretched for better viewing using ***View > Stretch Z…***



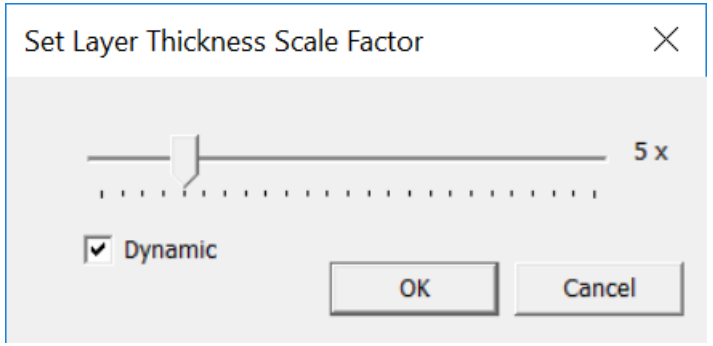
Properties

Name	Value	Unit
Type	Via	
LockPosition	☐	
Name	via_2029	
Net		
Padstack Definition	Solder_Template	
Padstack Usage	...	
Start Layer	AP	
Stop Layer	Metal5	
Backdrill Top	----	
Backdrill Bottom	----	
OverrideHoleDiam...	☐	
HoleDiameter	15	um
Location	0.2085652068949 ...	mm
Angle	0	deg

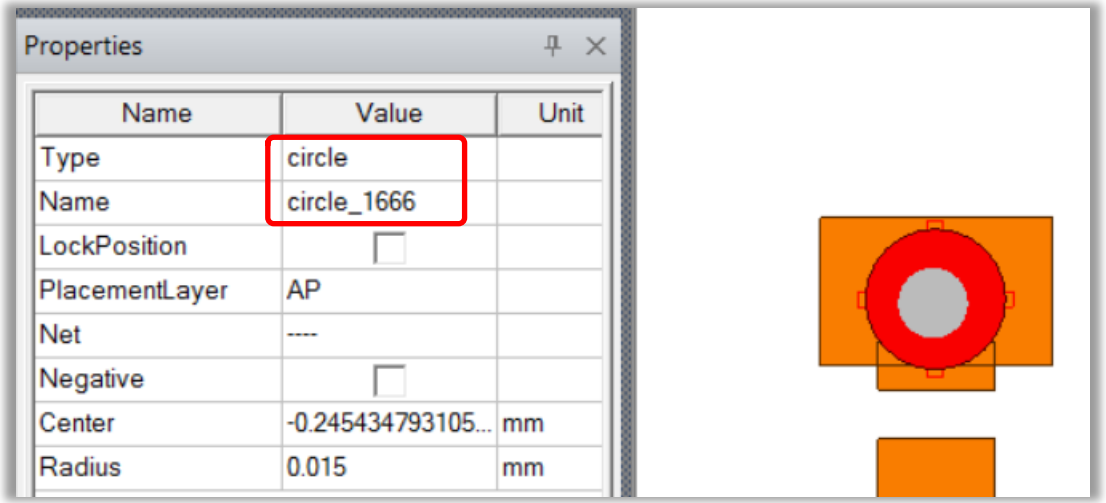


This is the second & lower via

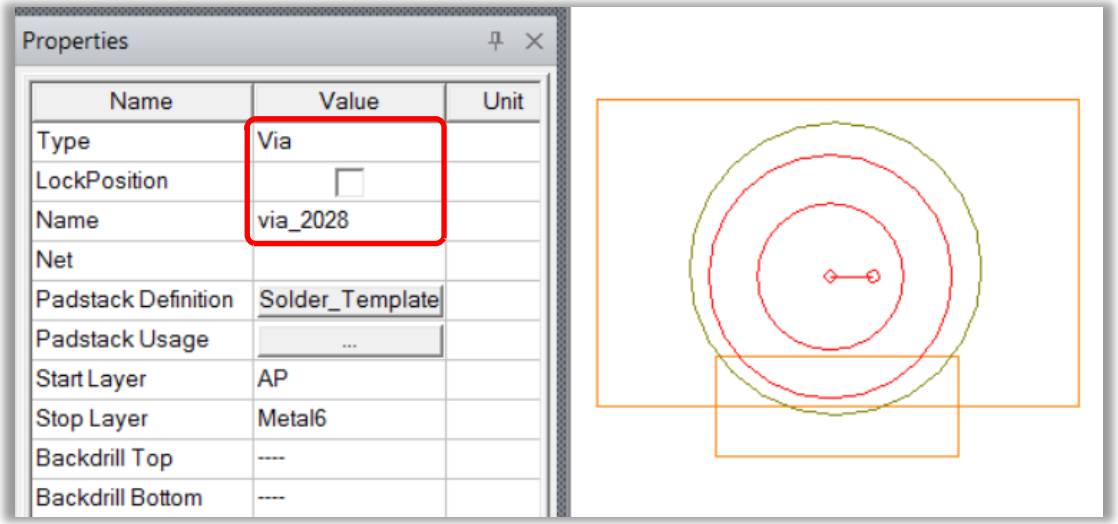
This is layer Metal5



Selecting the Via in the Circle - Display Sketch



In the top-down view, it is easy to point at the via and select the circle instead. One can verify what is selected by referring to the ***Properties***.

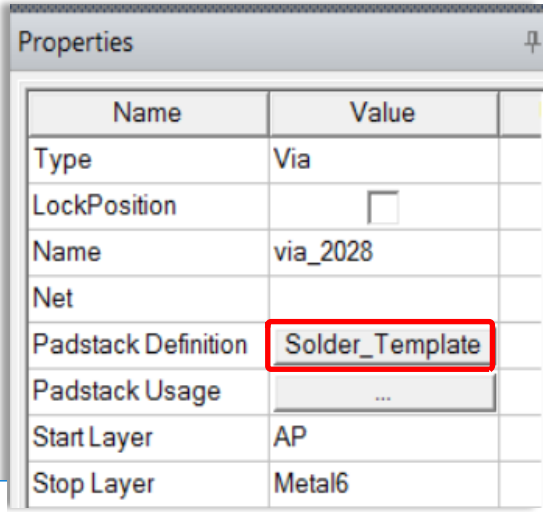


One good way to pick out and select a particular object, positioned close to other objects, is to use ***Display Sketch***. In this way we can point at and select exactly what we want. Then in ***Properties*** we can verify that we have selected what we want (the via in this case).

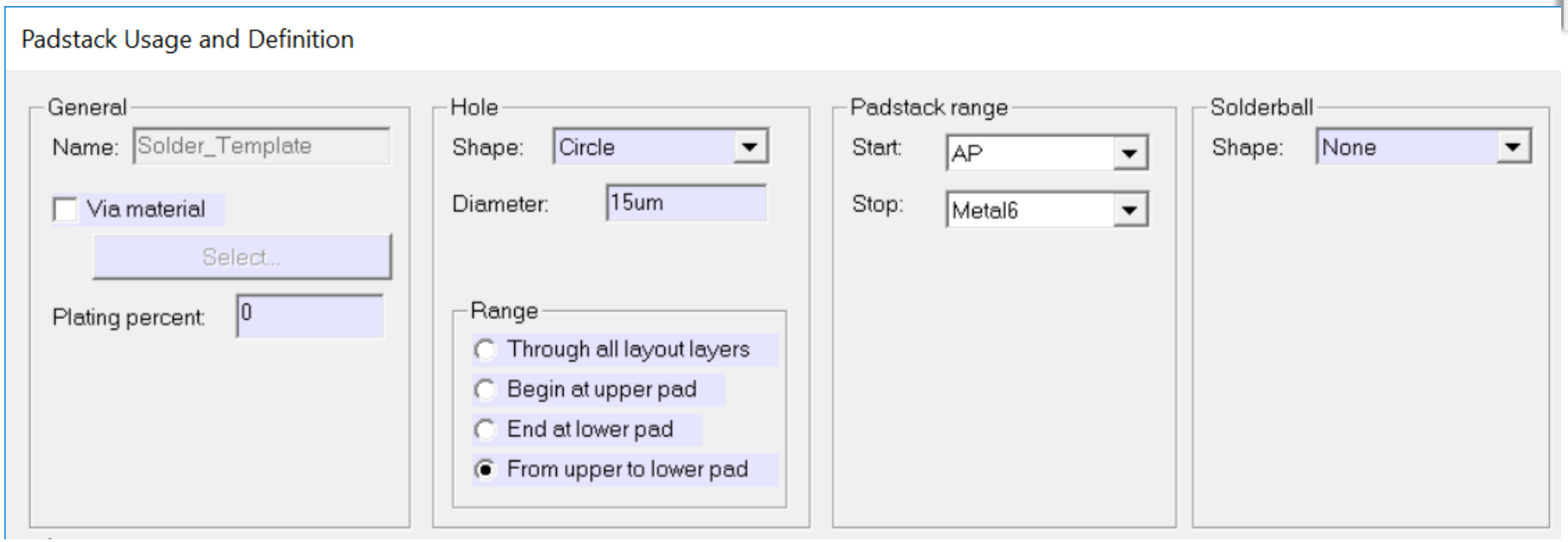
Create Solderball Reference on Top Via 1

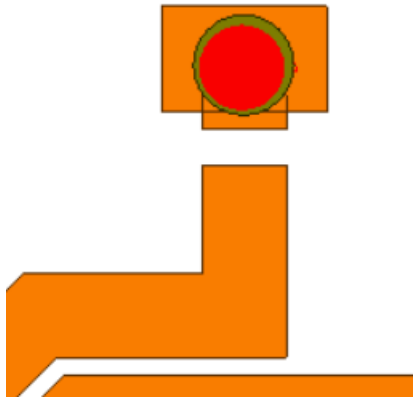
With one of the vias selected, in the ***Properties*** window:

- In the ***Padstack Usage*** line, under ***Value***, click on the button (which should show ellipses, three periods in a row), to bring up the ***Padstack Usage and Definition*** window.



Solder Ball properties are added to create the long vertical sections for the return path.





... initial view ... continued ...

Padstack Usage and Definition Window - OnChip_OctSpiralL1.aedt

In the ***Padstack Usage and Definition*** window

- Set ***Padstack Range***:
  - ***Start*: AP**
  - ***End*: Metal6**
- Solderball:
  - ***Shape*: Cylinder**
  - ***Diameter*: 12.5um**
  - ***Connection Layer*: BRD**
- Click the ***OK*** button, which brings up the ***Apply Padstack Definition Changes*** window

… continued …

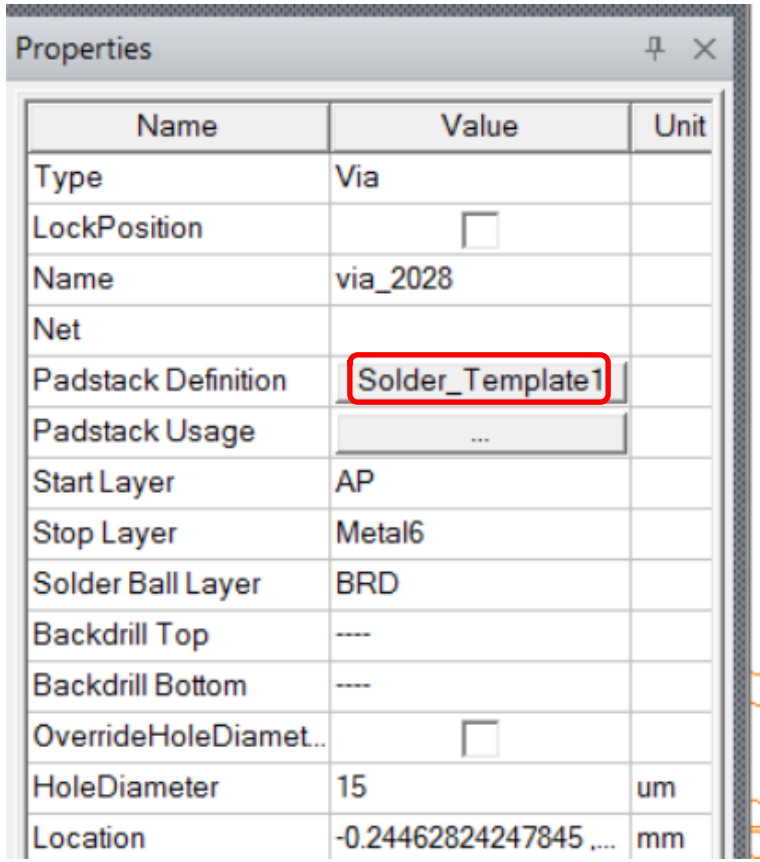
Finish Solderball Reference for Top Via 1

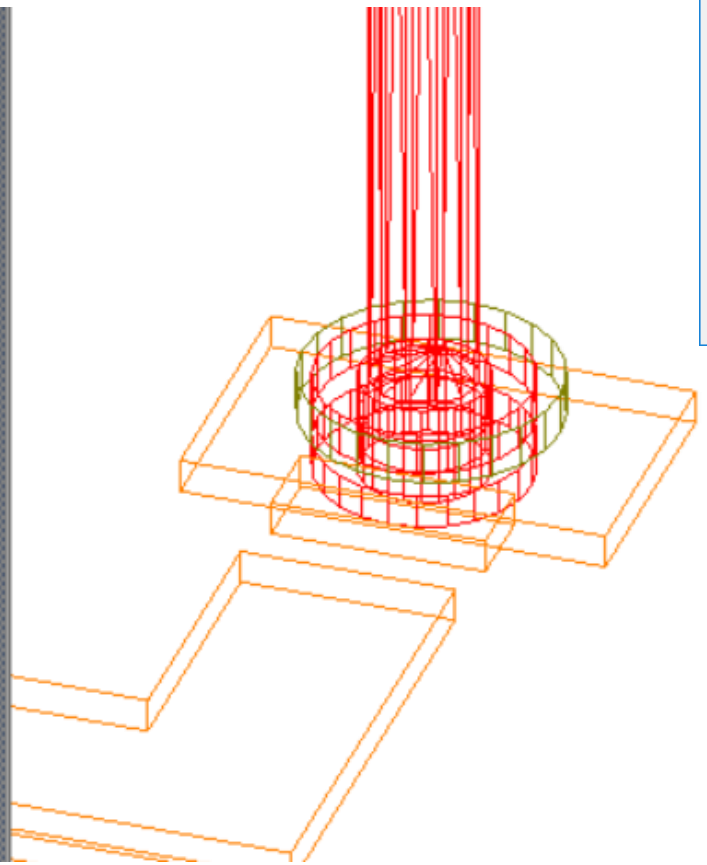
In the In ***Apply Padstack definition*** changes window…

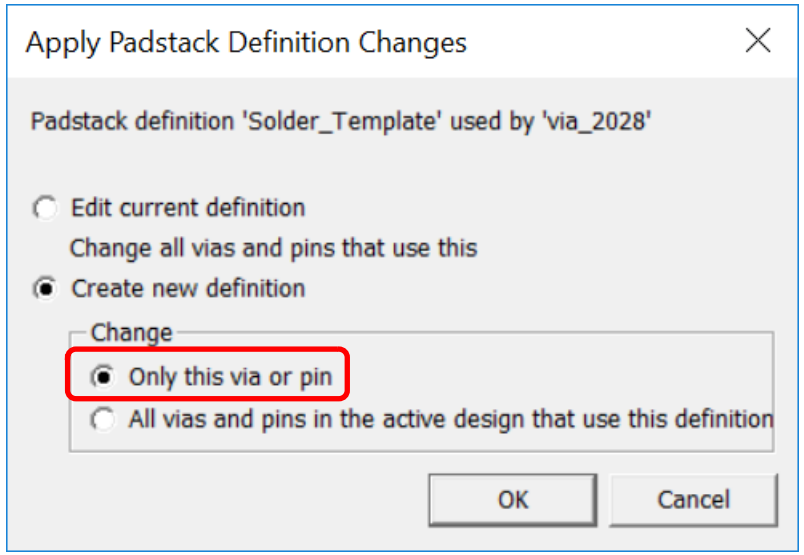
– Select ***Create new definition***

– Select ***Only this via or pin***

- Click the ***OK*** button







Notice how there is now a new ***Padstack Definition*** Solder_Template**1**.

Create Solderball Reference on Top Via 2

With one of the vias selected, in the ***Properties*** window:

- In the ***Padstack Usage*** line, under ***Value***, click on the button (which should show ellipses, three periods in a row), to bring up the ***Padstack Usage and Definition*** window.

Properties

Name	Value
Type	Via
LockPosition	
Name	via_2029
Net	
Padstack Definition	Solder_Template
Padstack Usage	...
Start Layer	AP
Stop Layer	Metal5

Solder Ball properties are added to create the long vertical sections for the return path.

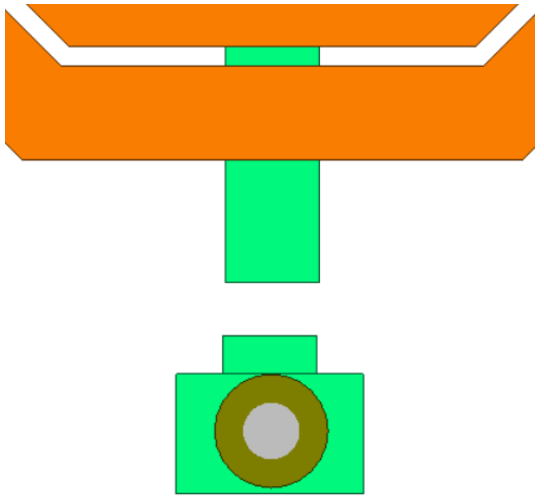
Padstack Usage and Definition

General
Name: Solder_Template
Via material
Select...
Plating percent: 0

Hole
Shape: Circle
Diameter: 15um
Range
Through all layout layers
Begin at upper pad
End at lower pad
From upper to lower pad

Padstack range
Start: AP
Stop: Metal5

Solderball
Shape: None



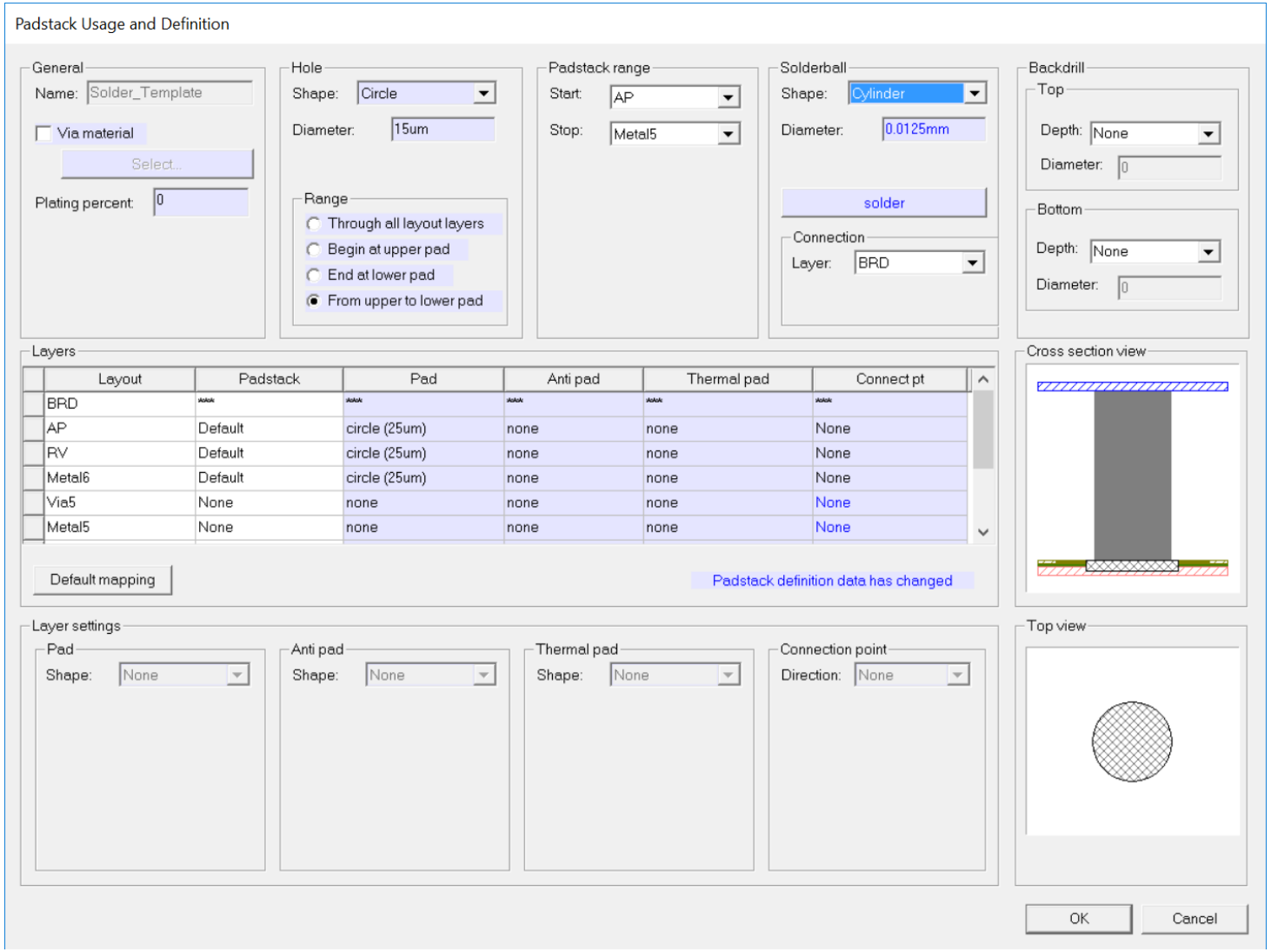
... initial view ... continued ...

Padstack Usage and Definition Window - OnChip_OctSpiralL1.aedt

In the ***Padstack Usage and Definition*** window

- Set ***Padstack Range***:
  - ***Start*: AP**
  - ***End*: Metal6**
- Solderball:
  - ***Shape*: Cylinder**
  - ***Diameter*: 12.5um**
  - ***Connection Layer*: BRD**
- Click the ***OK*** button, which brings up the ***Apply Padstack Definition Changes*** window

… continued …

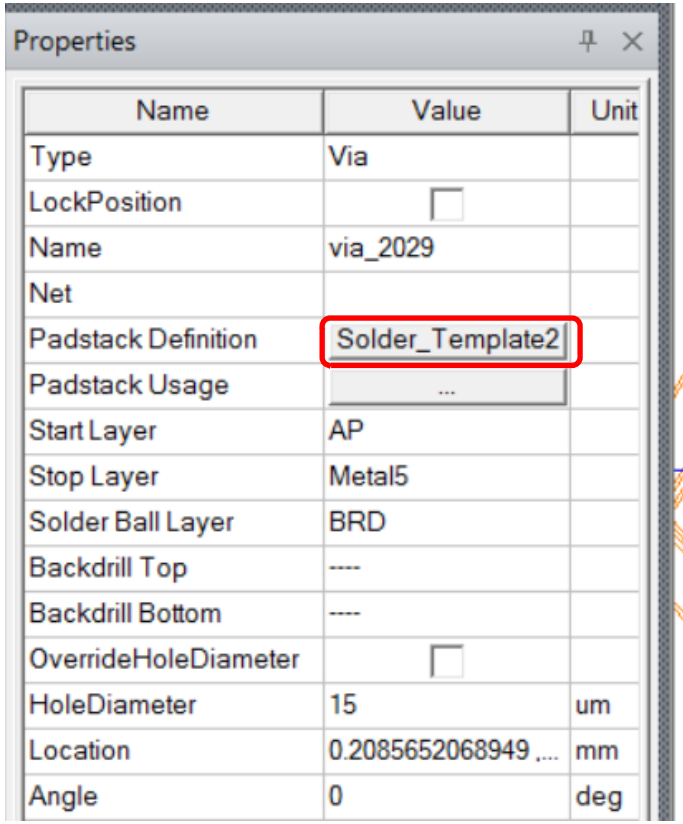


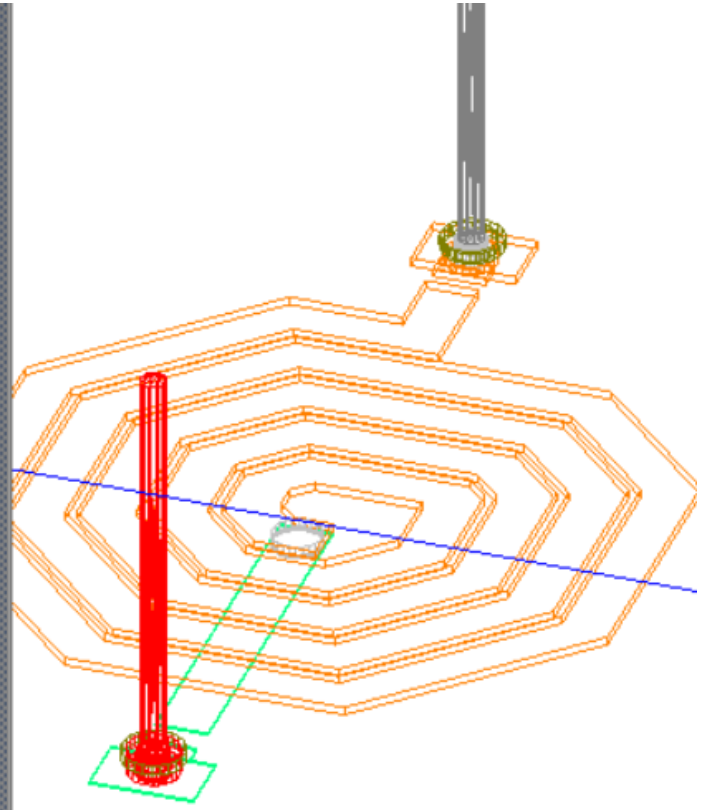
Create Solderball Reference for Bottom Via 2

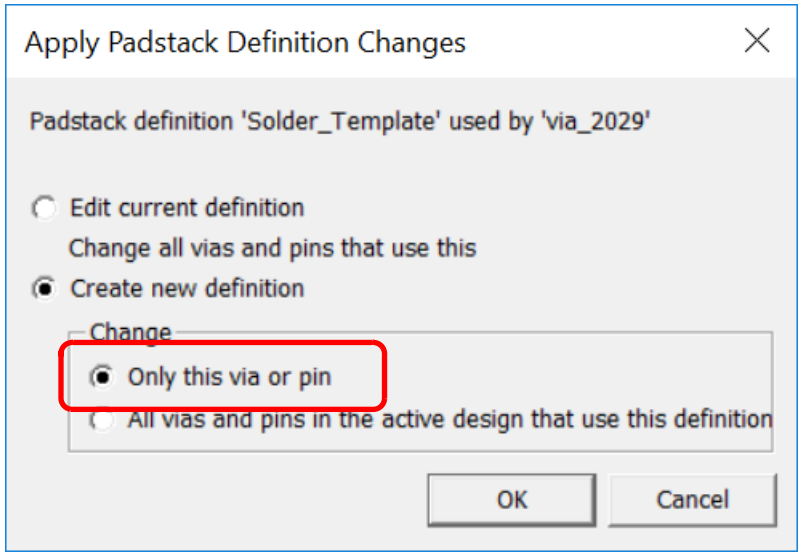
In the In ***Apply Padstack definition*** changes window…

- Select ***Create new definition***
- Select ***All vias and pins in the active design that use this definition***

- Click the ***OK*** button





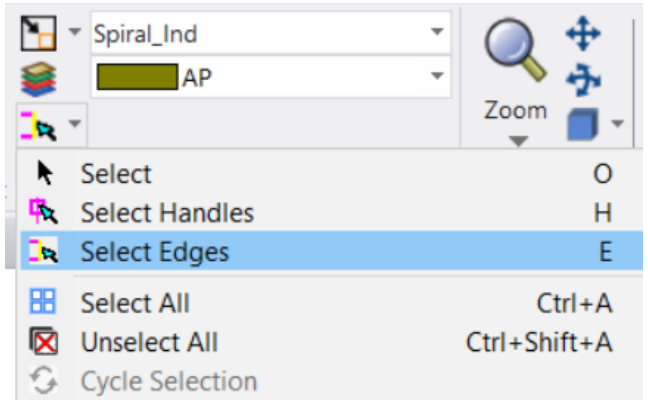


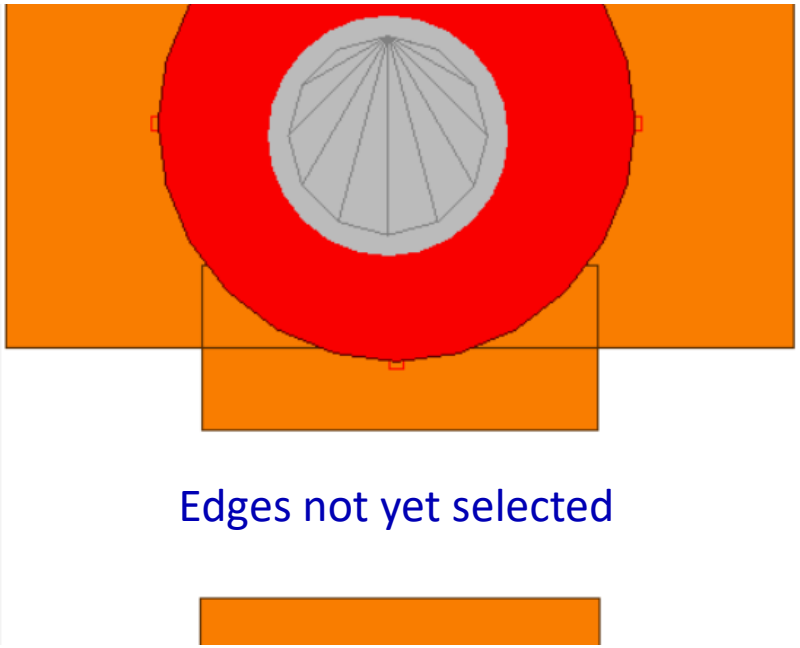
Notice how there is now a new ***Padstack Definition*** Solder_Template**2**.

Select Edges for First Gap Port at Top

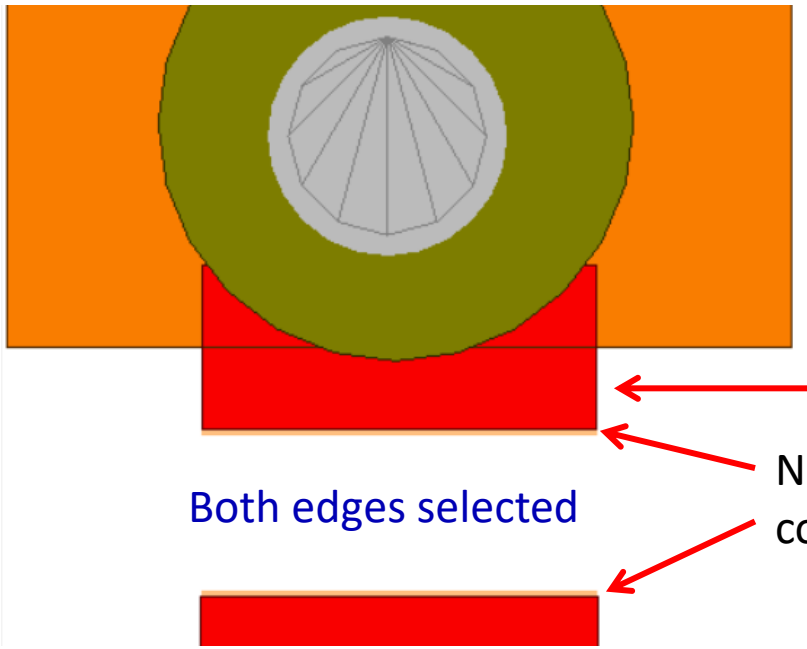
- In the ***Ribbon***, with the **Layout** tab selected, click on ***Select Edges*** (or just click the ***E*** key)
- Select the two edges on either side of the gap.
  This gap port will be horizontally oriented.

Select Edges mode cursor





Edges not yet selected



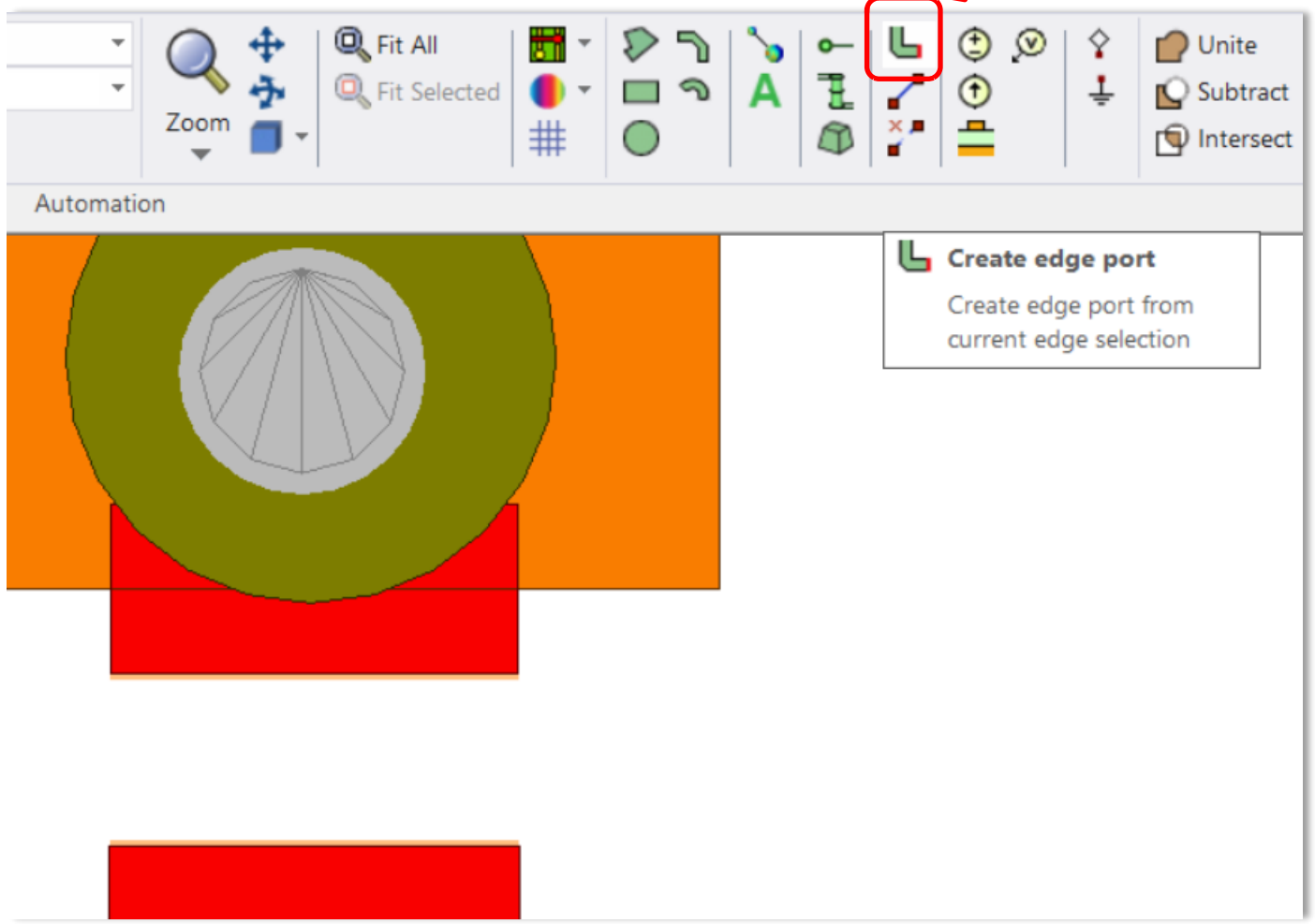
Both edges selected

Notice that the entire geometry changes color.

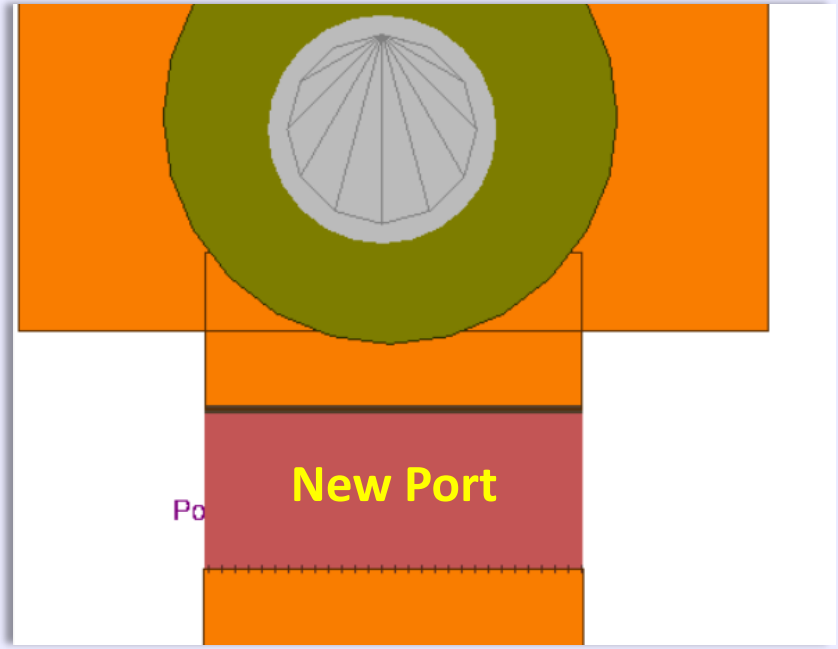
Notice the new color on the edges.

Create First Gap Port - OnChip_OctSpiralL1.aedt

- In the ***Ribbon***, with the **Layout** tab selected, click on ***Create Edge Port***



First Port Finished

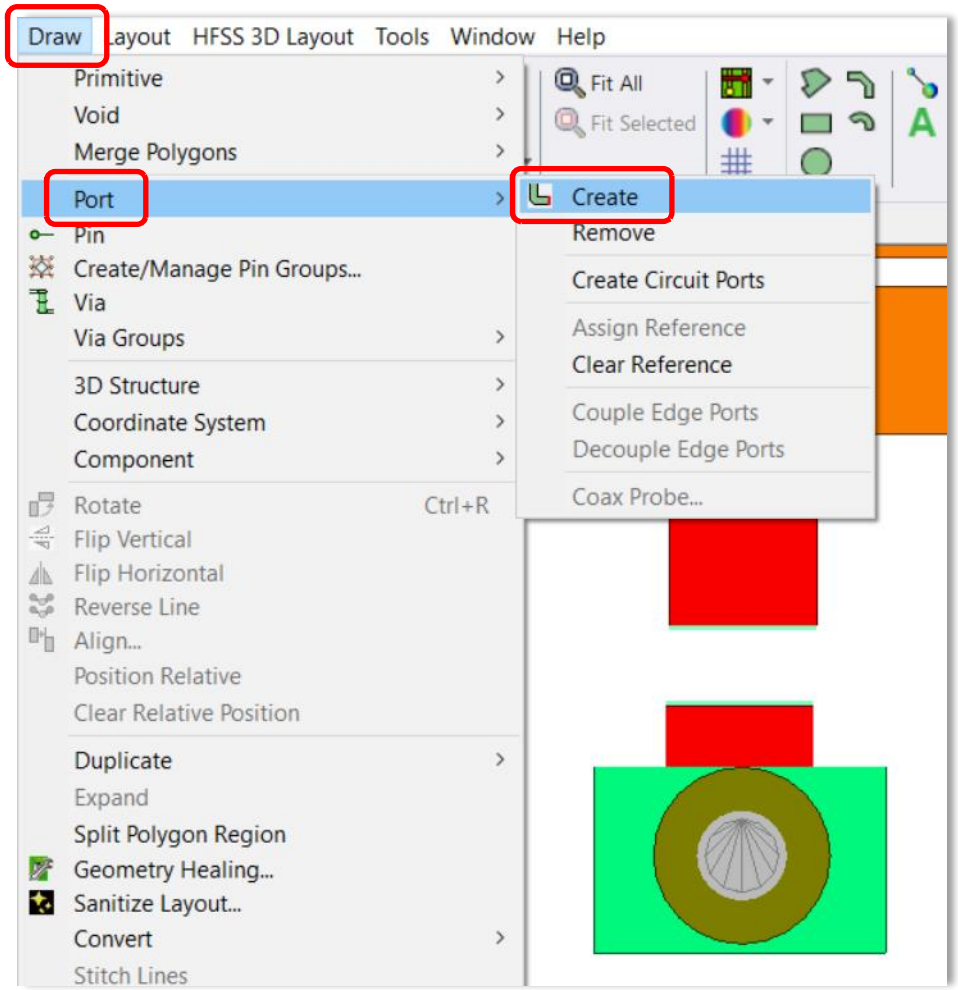


If the edge port rectangle does not appear, check ***Layout > Draw HFSS Ports***.

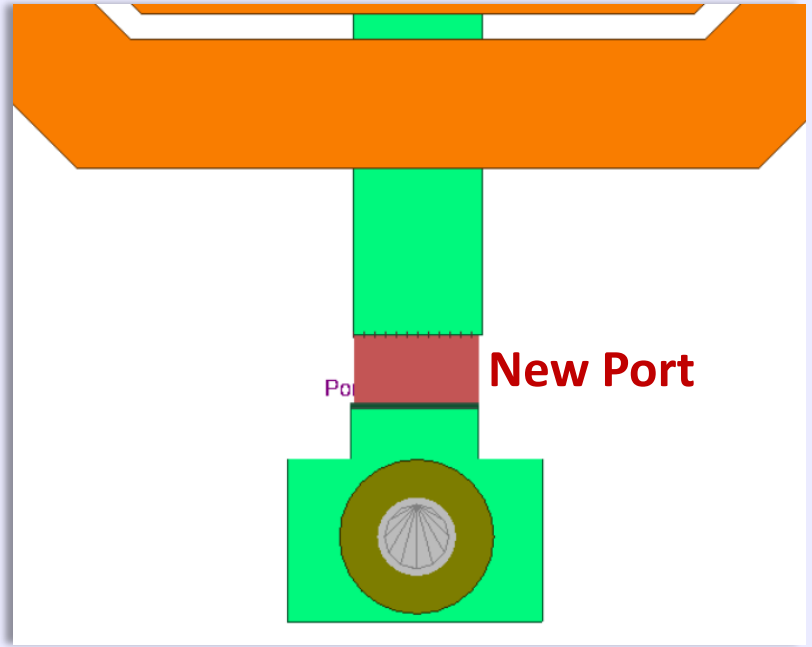
The new port should also appear in the ***Project Manager*** under ***Excitations***.

Create Second Gap Port at Bottom

- From the top of the GUI, select ***Draw > Port > Create.***



Second Port Finished

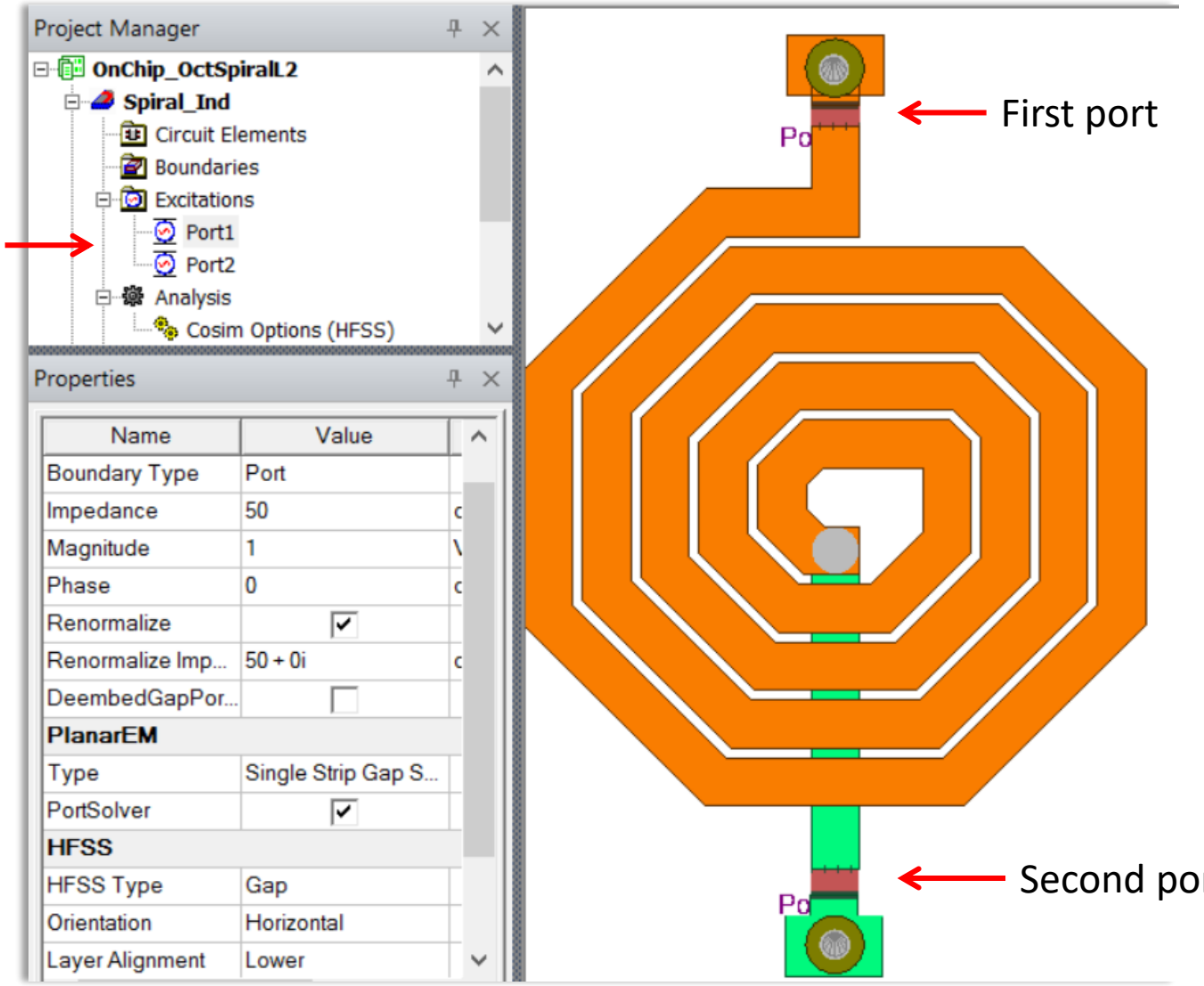


If the edge port rectangle does not appear, check ***Layout > Draw HFSS Ports***.

The new port should also appear in the ***Project Manager*** under ***Excitations***.

Both Ports Complete - OnChip_OctSpiralL2.aedt

Two ports



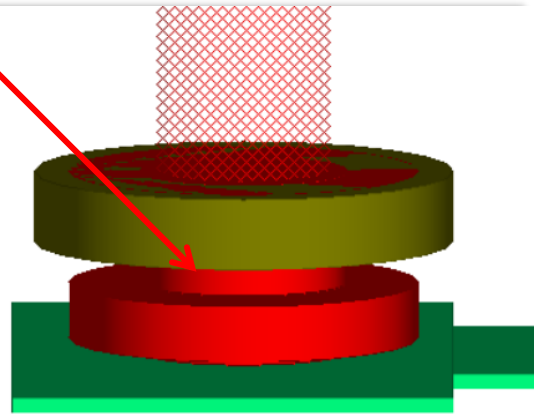
- Save project to **OnChip_OctSpiralL2.aedt**

Metal 5 and Metal 6 Final Via Stop Layer Check

Stop Layer Metal5

Properties

Name	Value	Unit	E...
Type	Via		
LockPosition	☐		
Name	via_2029		
Net			
Padstack Definit...	Solder_Templat...		
Padstack Usage	...		
Start Layer	AP		
Stop Layer	Metal5		
Solder Ball Layer	BRD		
Backdrill Top	----		
Backdrill Bottom	----		
OverrideHoleDi...	☐		
HoleDiameter	15	um	1...

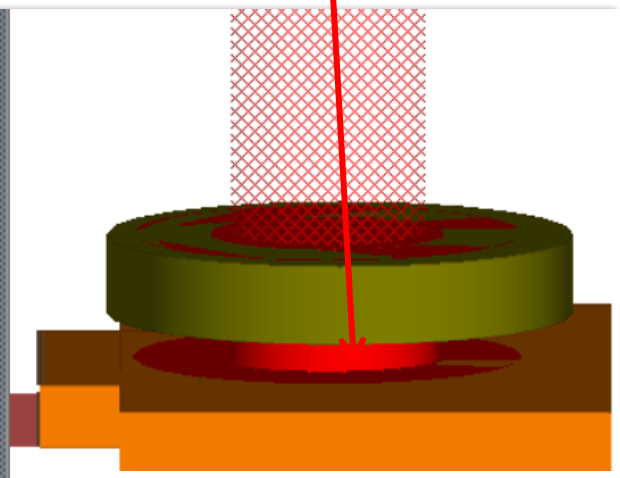


This green conductor is on layer Metal5.

Stop Layer Metal6

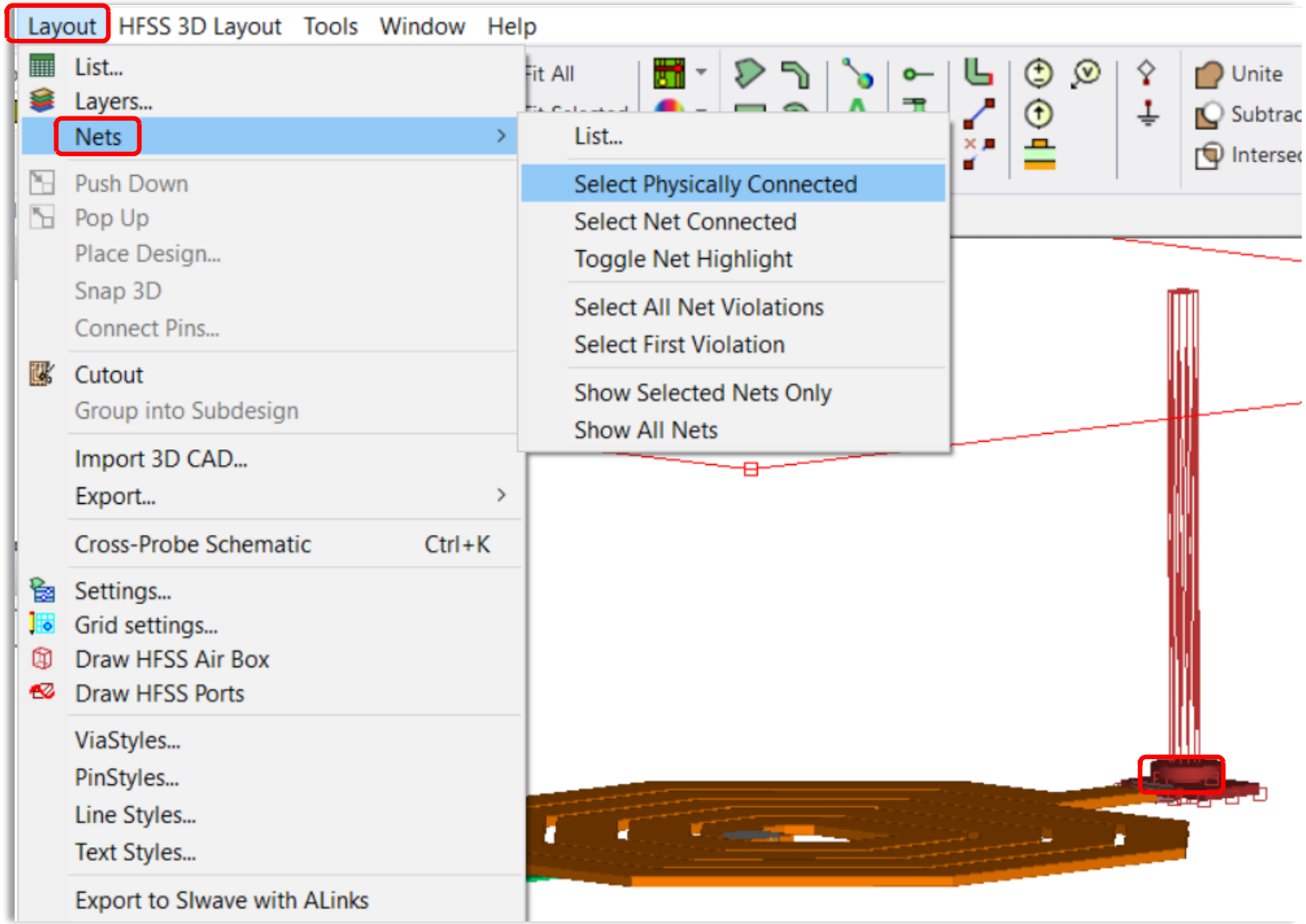
Properties

Name	Value	Unit	E...
Type	Via		
LockPosition	☐		
Name	via_2028		
Net			
Padstack Definit...	Solder_Templat...		
Padstack Usage	...		
Start Layer	AP		
Stop Layer	Metal6		
Solder Ball Layer	BRD		
Backdrill Top	----		
Backdrill Bottom	----		

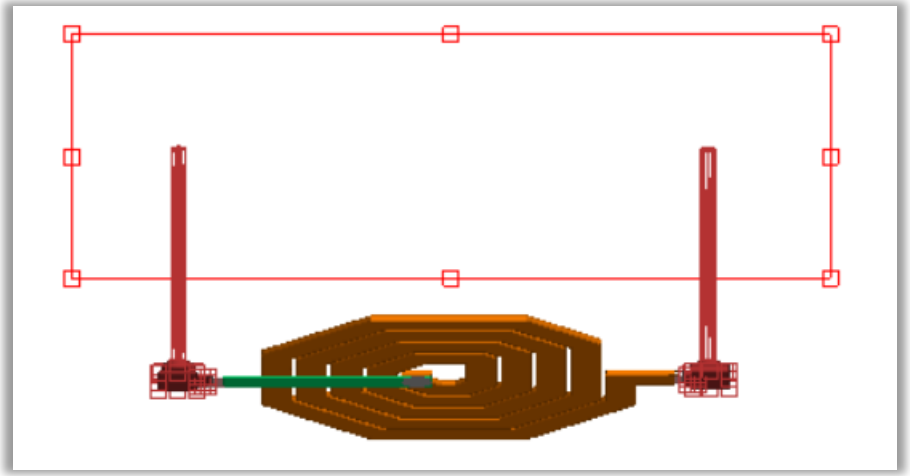


This orange conductor is on layer Metal6.

DC Continuity Check - Select Physically Connected



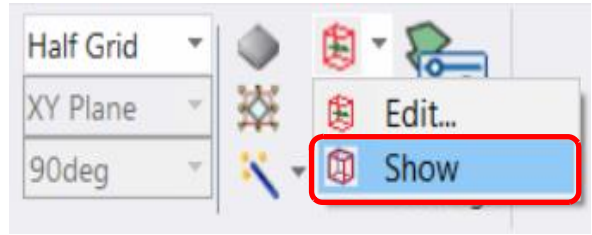
A good way to check or troubleshoot a design is checking the DC continuity through ***Layout > Nets > Select Physically Connected***.

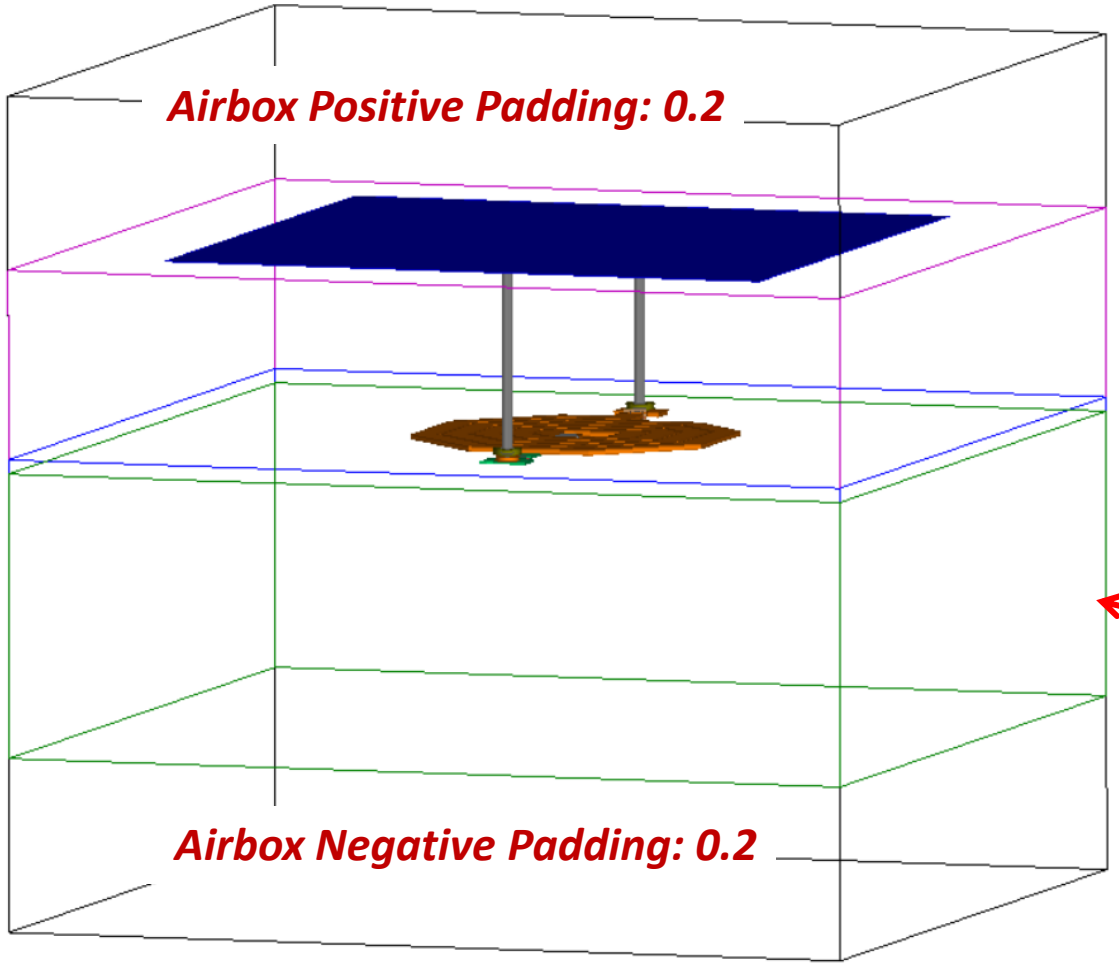


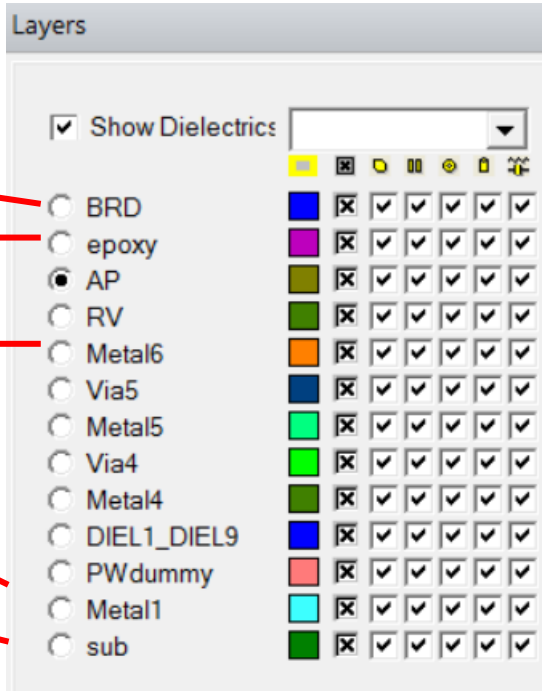
In these pictures we're checking that the vias are all connected in a DC path from port to port through layer **BRD**. The spiral is not part of this.

View HFSS Extents - OnChip_OctSpiralL2.aedt

- In the ***Ribbon***, with the **Layout** tab selected, on the far right, click on the ***Extents*** icon and select ***Show*** (if the ***Extents*** airbox is not already showing).



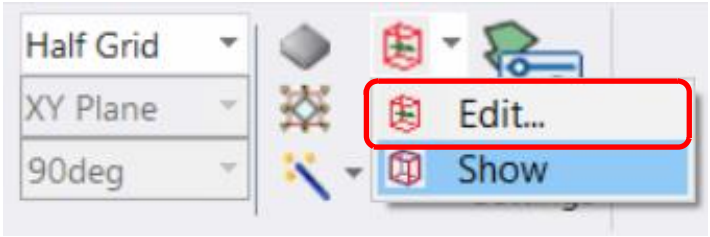


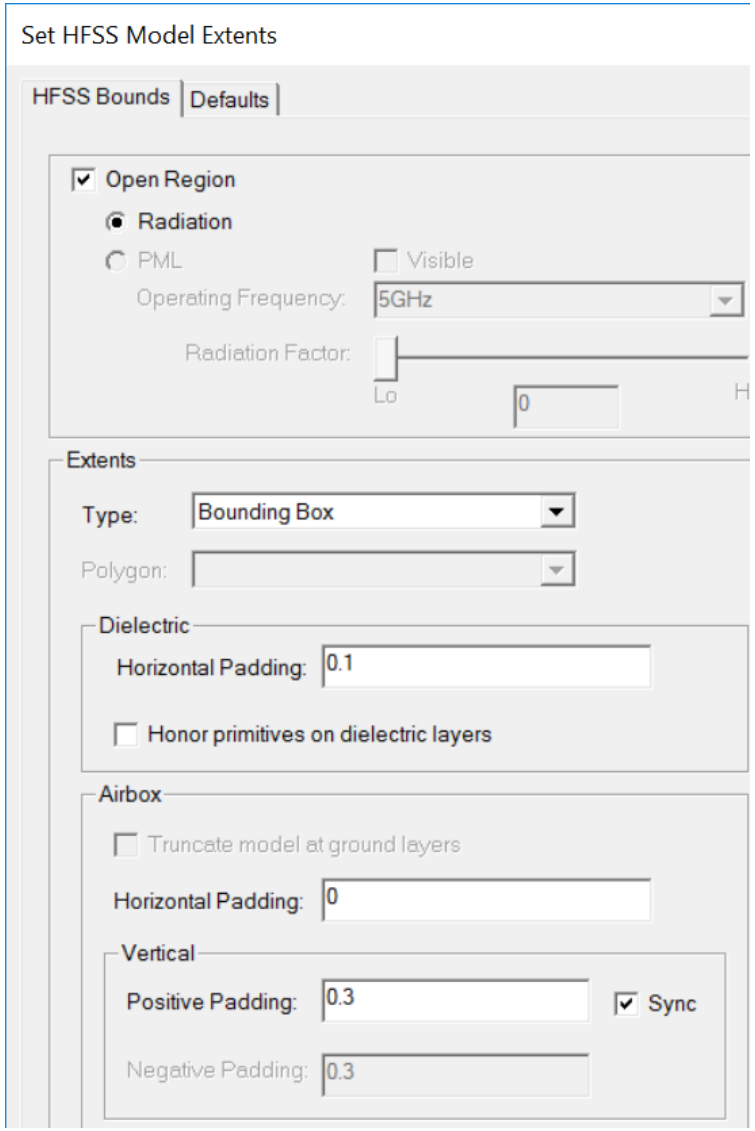


HFSS Extents defines the meshed simulation volume of the finite element method (FEM) 3D simulation. Horizontal Padding can also define the substrate dielectric size.

Edit HFSS Extents

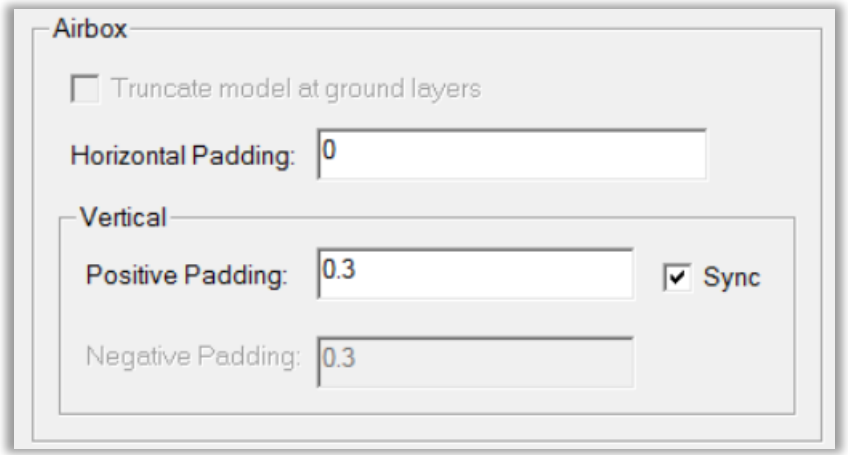
- In the ***Ribbon***, with the **Layout** tab selected, on the far right, click on the ***Extents*** icon and select ***Edit*** to bring up the ***Set HFSS Model Extents*** dialog window.



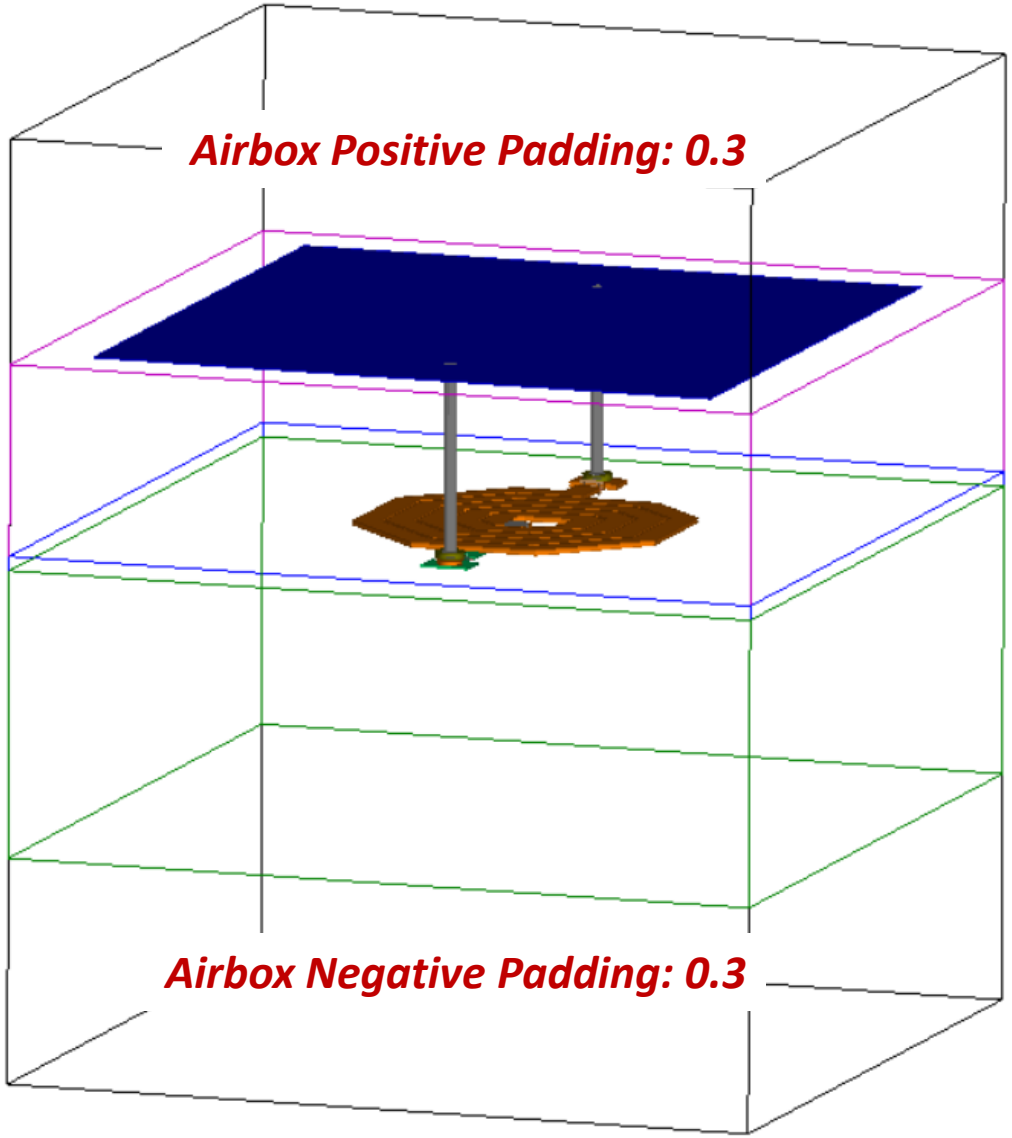


- Set …
  1. ***Dielectric*** section:
     - ***Horizontal Padding***: **0.1**
  2. ***Airbox*** section
     - ***Horizontal Padding***: **0**
     - ***Vertical Padding***: **0.3**
     - ***Sync***: ☑
  3. Click the ***OK*** button to close the window.

View Final Edited HFSS Extents



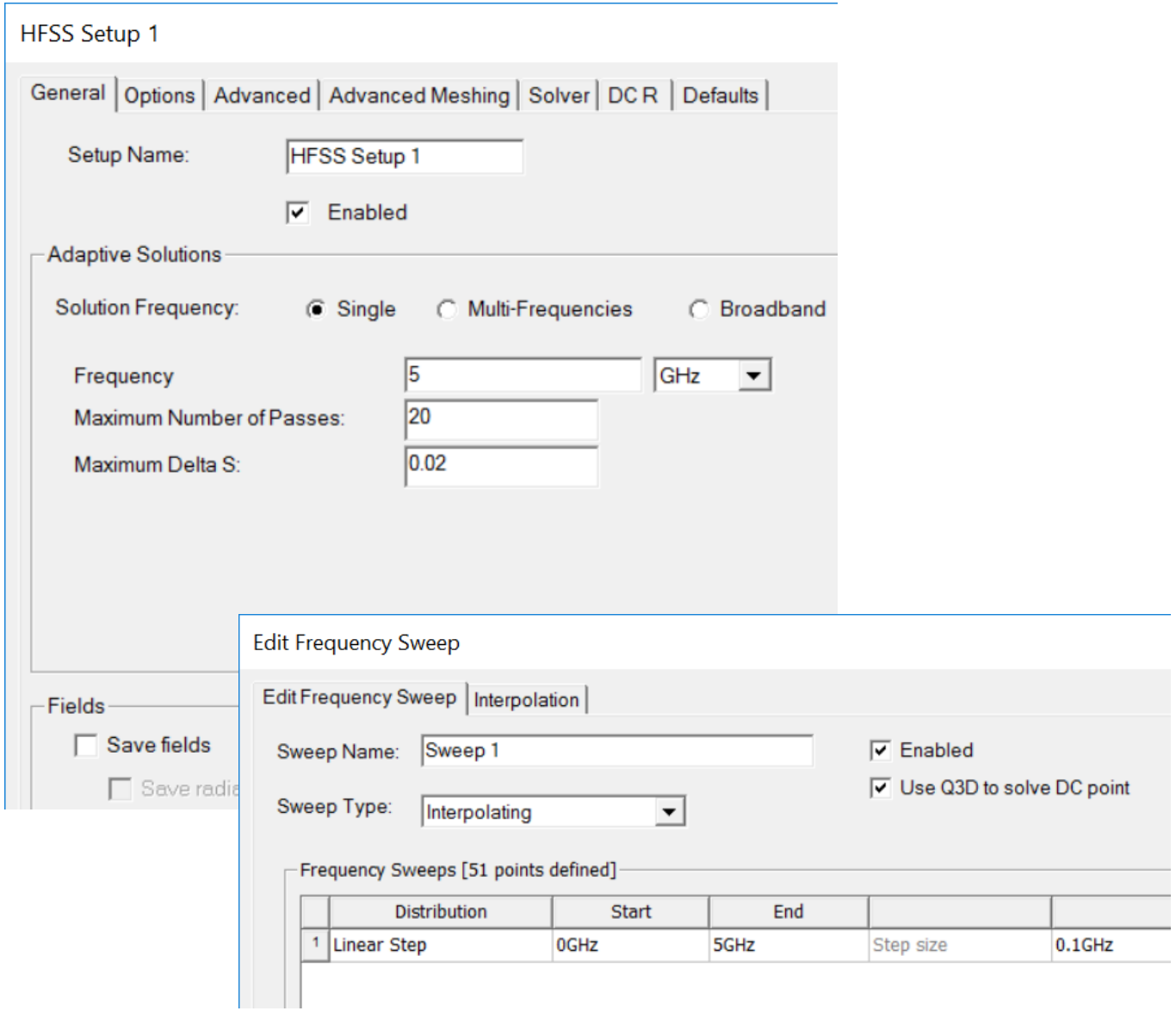
The ***Sync*** checkbox synchronizes the ***Airbox Negative Padding*** with the ***Positive Padding***.



Create HFSS Solution Setup

- In the ***Project Manager***, right-click on ***Analysis*** and select ***Add HFSS Solution Setup***
  1. Click the ***General*** tab:
     - ***Setup Name***: **HFSS Setup1**
     - ***Solution Frequency***: **5 GHz**
     - ***Maximum Number of Passes***: **20**
     - ***Maximum Delta S***: **0.02**
     - ☐ ***Save fields***
  2. Click the ***OK*** button

  The frequency sweep setup dialog will automatically appear
- In the ***Edit Frequency Sweep*** tab dialog box
  1. ***Name***: **Sweep 1**
  2. ☑ **Use Q3D to solve DC point**
  3. ***Sweep Type***: ***Interpolating***
  4. Specify ***Frequency Sweeps*** section
     - ***Distribution***: ***Linear Step***
     - ***Start***: **0 GHz**
     - ***Stop***: **5 GHz**
     - ***Step***: **0.1 GHz**
  5. Press the ***OK*** button



Output Variables for Inductance and Quality Factor Plots

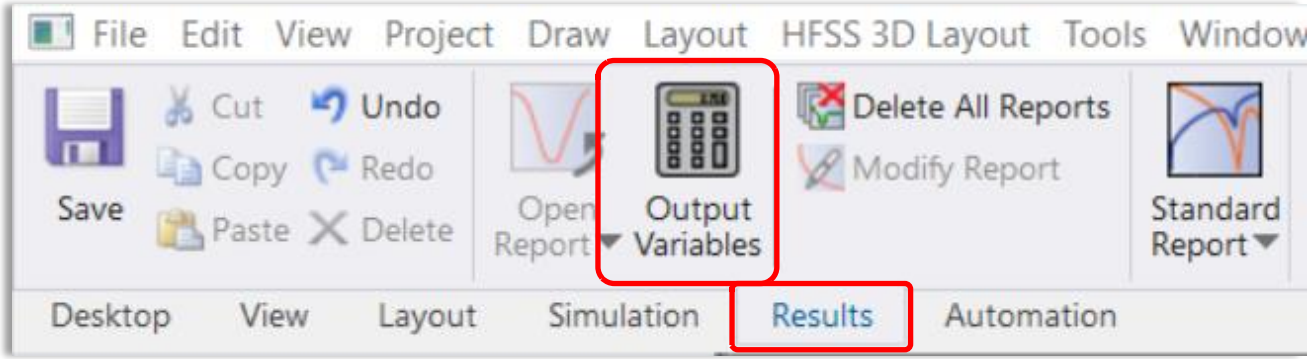
Equations for the inductance of a spiral inductor, often expressed in terms of Y-parameters, depend upon the configuration of the spiral inductor ports. In order to facilitate the ability to plot many calculated quantities, like inductance and quality factor Q, we can define equations as ***Output Variables*** for HFSS to plot in ***Reports***.

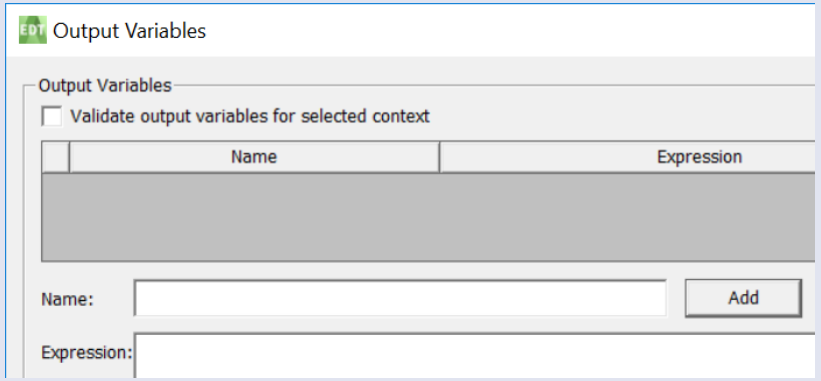
$$L = \frac{im\left(\frac{1}{Y_{11}}\right)}{2\pi f}$$

$$Q = abs\left(\frac{im\left(\frac{1}{Y_{11}}\right)}{re\left(\frac{1}{Y_{11}}\right)}\right)$$

- To access the ***Output Variables*** definitions, in the ***Ribbon***, with the Results tab selected, click on the ***Output Variables*** icon.

  *(Or … alternatively … from the top menu select item **HFSS 3D Layout > Results > Output Variables...**)*



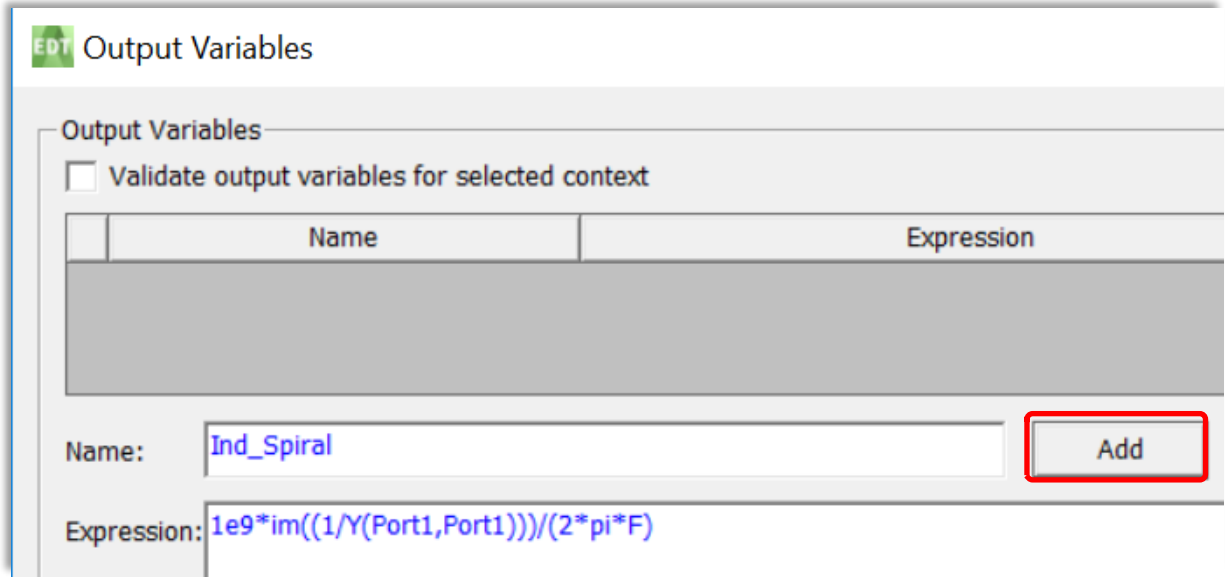


Expression is the equation of interest and ***Name*** is what appears in the ***Report*** window for plotting.

Creating an Output Variable for Inductance - Ind_Spiral

- Bring up the ***Output Variables*** window and set:
  - ***Name*** box: Enter **Ind_SpiralA**
  - ***Expression*** box, type **1e9*im((1/**
    - ***Category***: Select ***Y Parameter*** from the drop-down box
    - ***Quantity***: **Y(Port1, Port1)**
    - Click the ***Insert into Expression*** button
  - In the Expression box, type: **))/(2*pi*F)**
  - Final Expression**:**
    1e9*im((1/Y(Port1, Port1)))/(2*pi*F)
  - Click the ***Add*** button

$$L = \frac{im\left(\frac{1}{Y_{11}}\right)}{2\pi f}$$

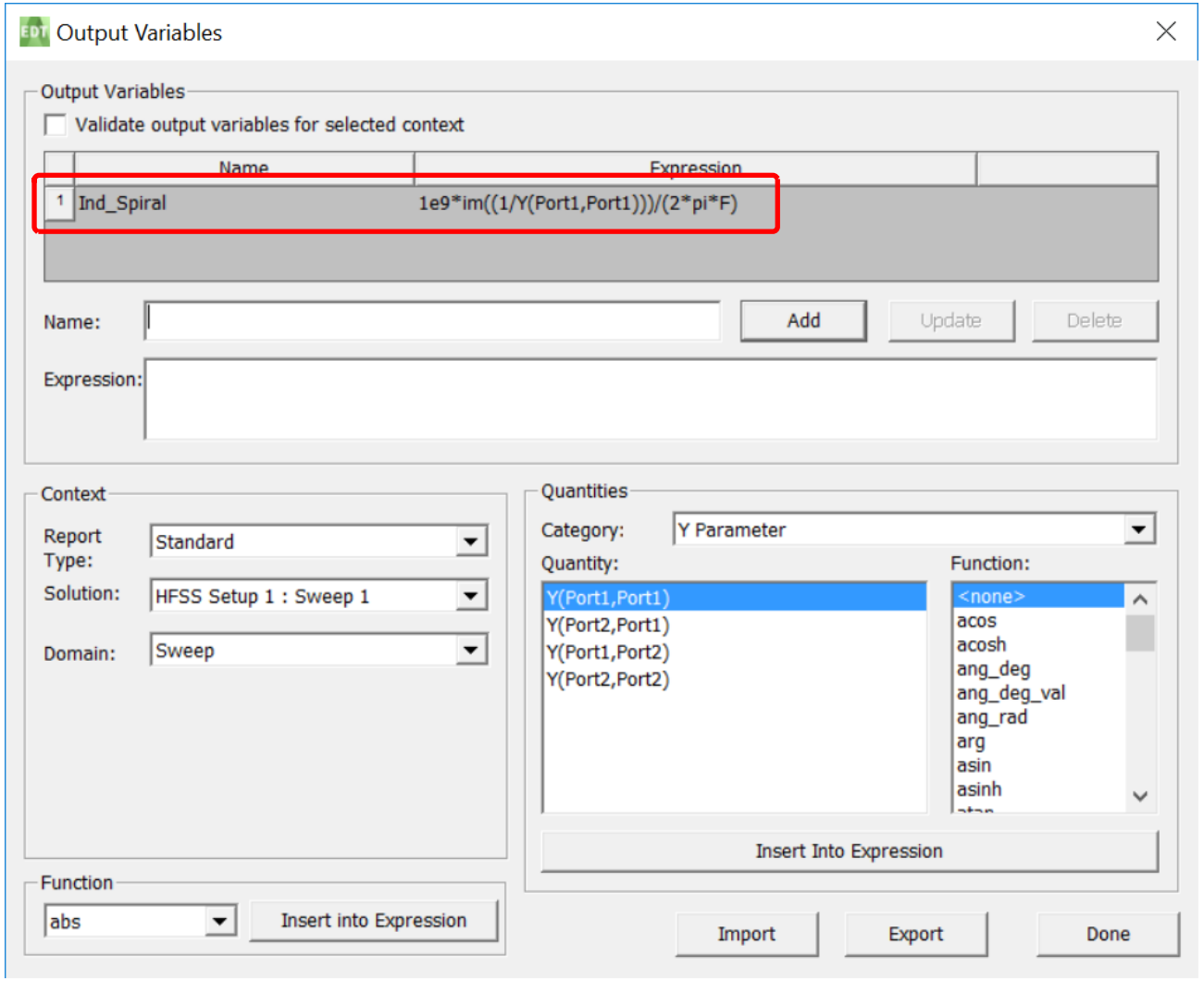


1e9: Inductance will be reported will be in **nH**
'**pi**' is a constant variable which is pre-defined
'**F**' is an intrinsic variable defined for the **Frequency**

Finished Output Variable for Inductance - Ind_Spiral

Ind_Spiral will be a signal available to the ***Results*** to plot in ***Reports.***

$$L = \frac{im\left(\frac{1}{Y_{11}}\right)}{2\pi f}$$



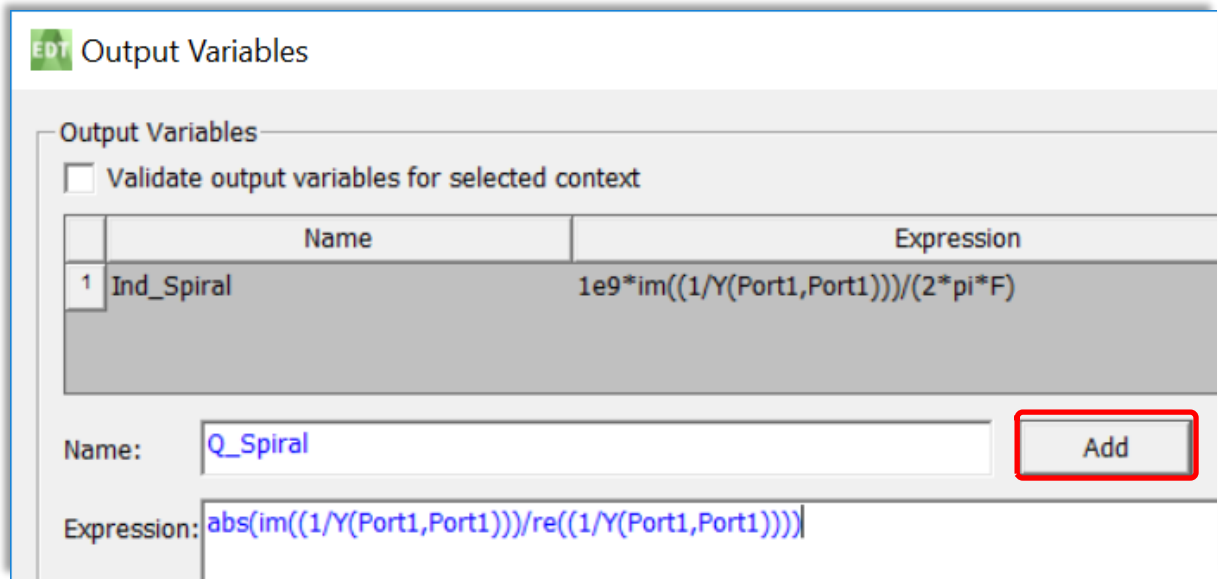
Creating an Output Variable for Quality Factor - Q_Spiral

- Bring up the ***Output Variables*** window and set:
  - ***Name*** box: Enter **Q_SpiralA**
  - ***Expression*** box, type **abs(im((1/**
    - ***Category***: Select ***Y Parameter*** from the drop-down box
    - ***Quantity***: **Y(Port1, Port1)**
    - Click the ***Insert into Expression*** button
  - ***Expression*** box, type: **))/re((1/**
    - ***Category***: Select ***Y Parameter*** from the drop-down box
    - ***Quantity***: **Y(Port1, Port1)**
    - Click the ***Insert into Expression*** button
  - ***Expression*** box, type: **))**
  - Final Expression**:**

abs(im((1/Y(Port1,Port1)))/re((1/Y(Port1,Port1))))

Click the ***Add*** button

$$Q = abs\left(\frac{im\left(\frac{1}{Y_{11}}\right)}{re\left(\frac{1}{Y_{11}}\right)}\right)$$

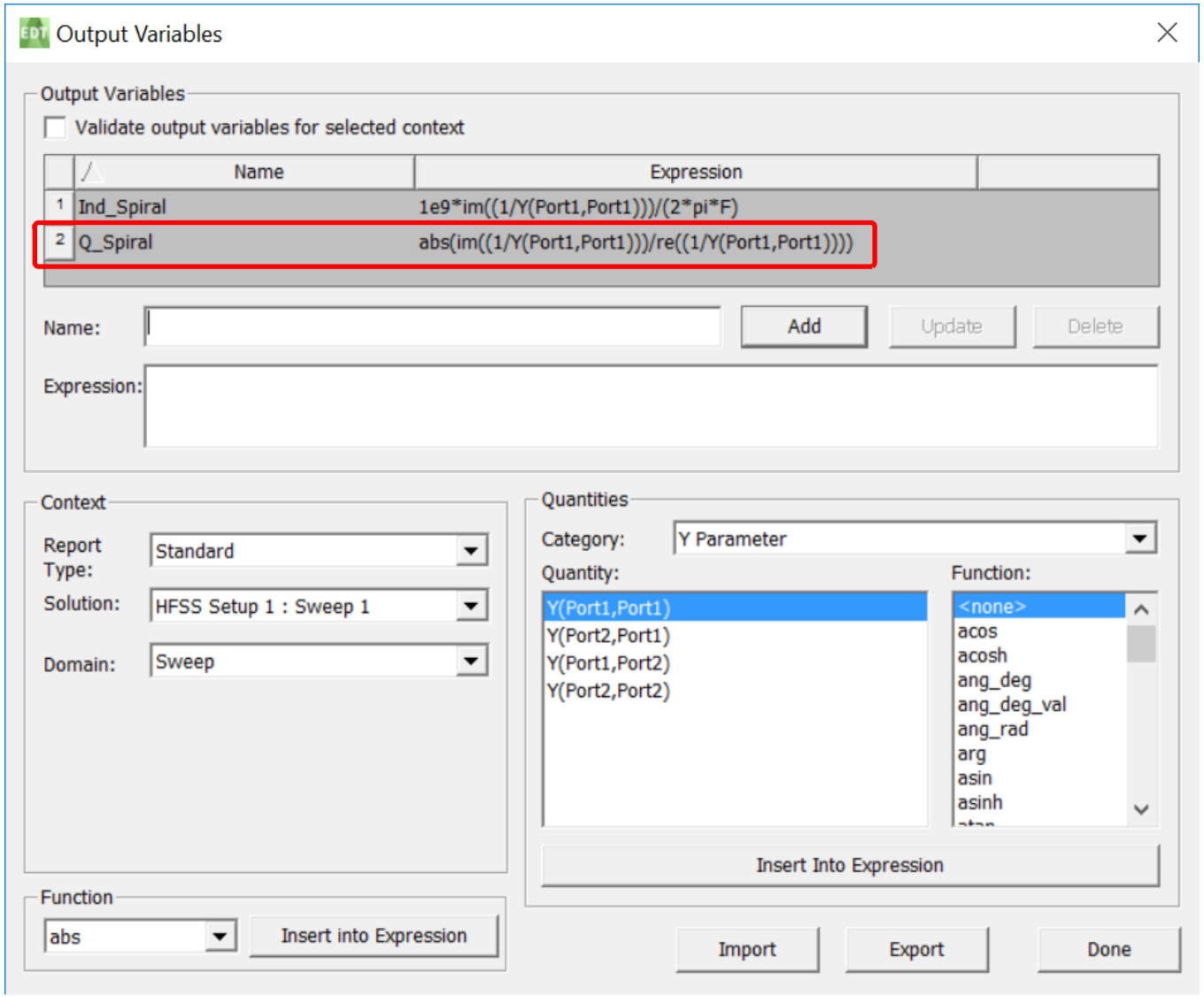


1e9: Inductance will be reported will be in **nH**
'**pi**' is a constant variable which is pre-defined
'**F**' is an intrinsic variable defined for the **Frequency**

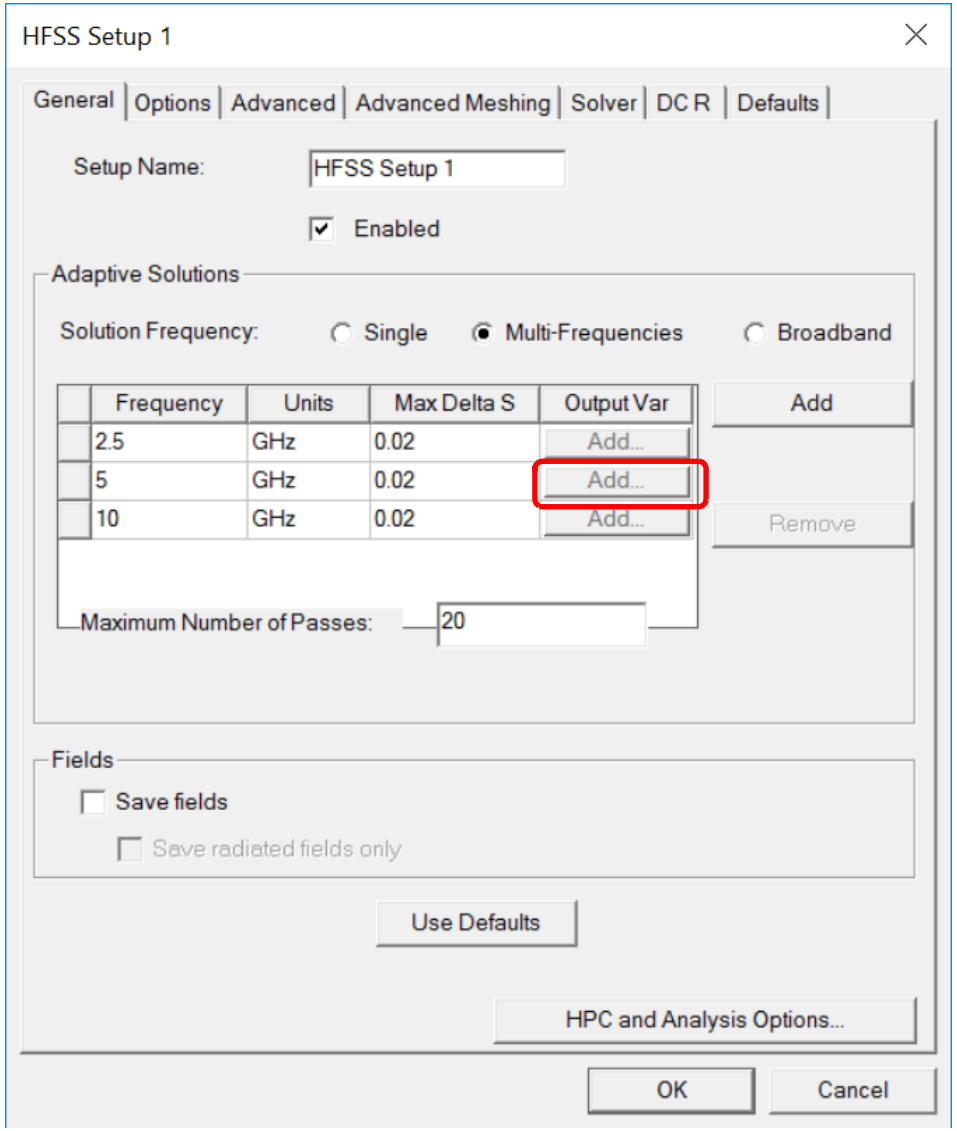
Finished Output Variable for Q - Q_Spiral - OnChip_OctSpiralL2.aedt

Q_Spiral will be a signal available to the ***Results*** to plot in ***Reports.***

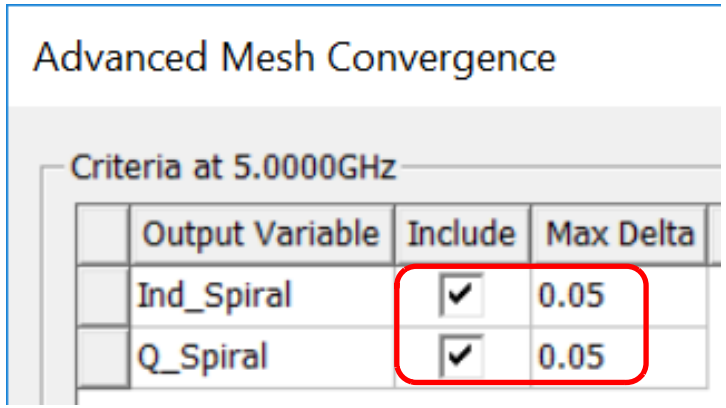
$$Q = abs\left(\frac{im\left(\frac{1}{Y_{11}}\right)}{re\left(\frac{1}{Y_{11}}\right)}\right)$$



Modify *Solution Setup* to Add *Output Variable* Mesh Convergence

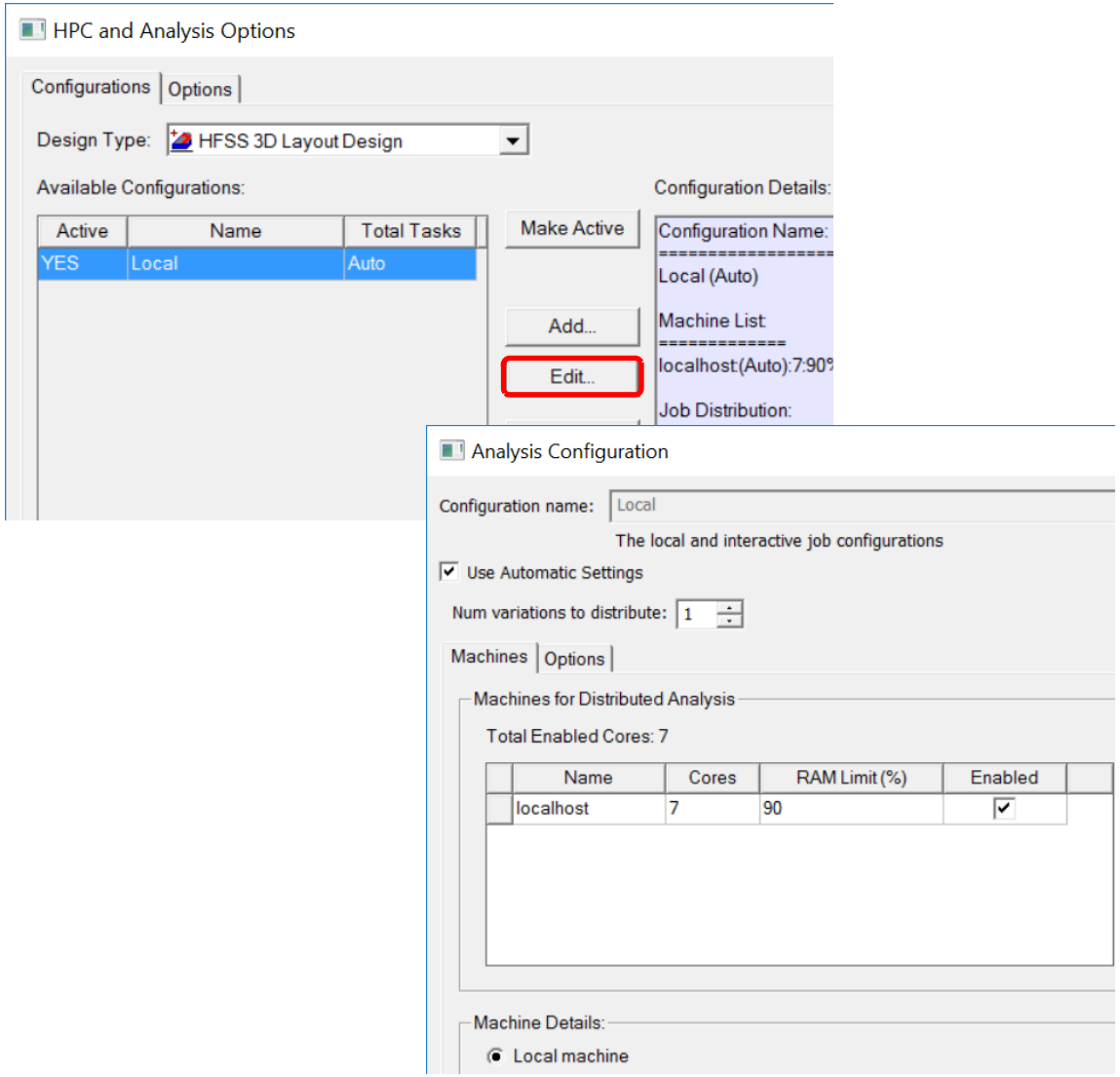


- Modify existing ***HFSS Solution Setup***:
  - In the ***Project Manager***, under ***Analysis***, double-click on the ***HFSS Setup 1*** to bring up the ***Solution Setup*** tab dialog box.
  - Under ***General*** tab, check ***Multi-Frequencies*** radio button
    - On the **5 GHz** line, below the ***Output Var*** column, click the ***Add...*** button
    - Include ☑ for all the ***Output Variables***
    - Max. Delta = **0.05** for Inductance and **0.05** for Quality factor.
  - Click the ***OK*** button twice in a row to close both windows.



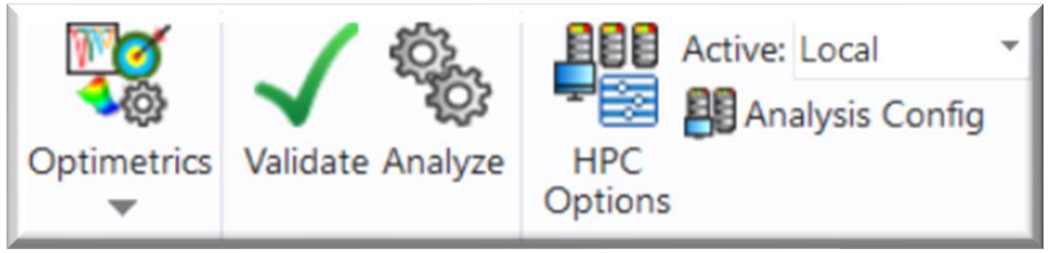
HPC Setup - OnChip_OctSpiralL3.aedt

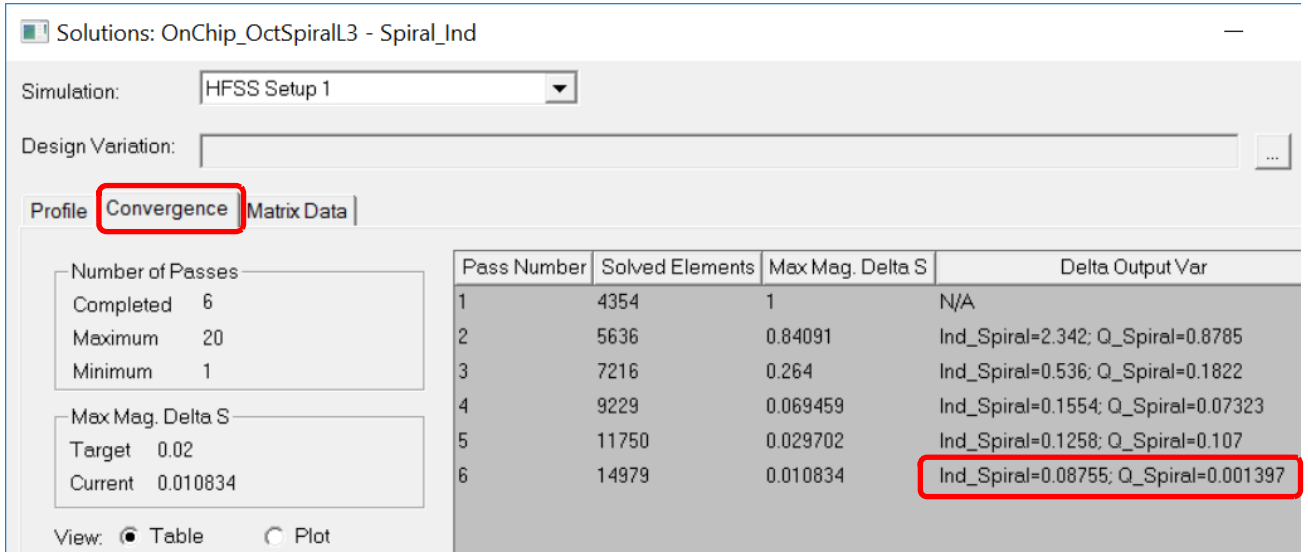
- Save Project **to OnChip_OctSpiralL3.aedt**
- In the ***Ribbon***, with the Simulation tab selected, click on the icon ***HPC Options*** to bring up the ***HPC and Analysis Options*** tab dialog box.
  - ***Design Type***: **HFSS 3D Layout Design**
  - Select the ***Active Configuration***: ***Local***
  - In the middle of the window, click on the ***Edit*** button to open the ***Analysis Configuration*** window.
- In the ***Analysis Configuration*** window …
  - Check the option for ***Use Automatic Settings***
  - Click the ***Machines*** tab
    - ***Name***: ***localhost***
    - ***Cores***: **4** (or **7** if 8 cores are available)
    - ***RAM Limit*** (%): **90**
    - Click the ***OK*** button to close ***Analysis Configuration***
  - Click the ***OK*** button to close ***HPC and Analysis Options***



Validate and Simulate OnChip_OctSpiralL3.aedt

- Save the project **OnChip_OctSpiralL3.aedt**.
- In the ***Ribbon***, with the **Simulation** tab selected, click on the green check mark to validate the simulation.
- Click on ***Analyze*** to start the simulation.
- In the ***Project Manager***, even while the simulation is running, under ***Analysis***, right-click on the HFSS Solution Setup and select ***Profile***
  - To view the ***Profile***, click the ***Profile*** Tab
  - To view the ***Convergence***, click the ***Convergence*** Tab
  - To view the ***Matrix Data***, click the ***Matrix Data*** Tab
- Press the ***Close*** button when you are finished.

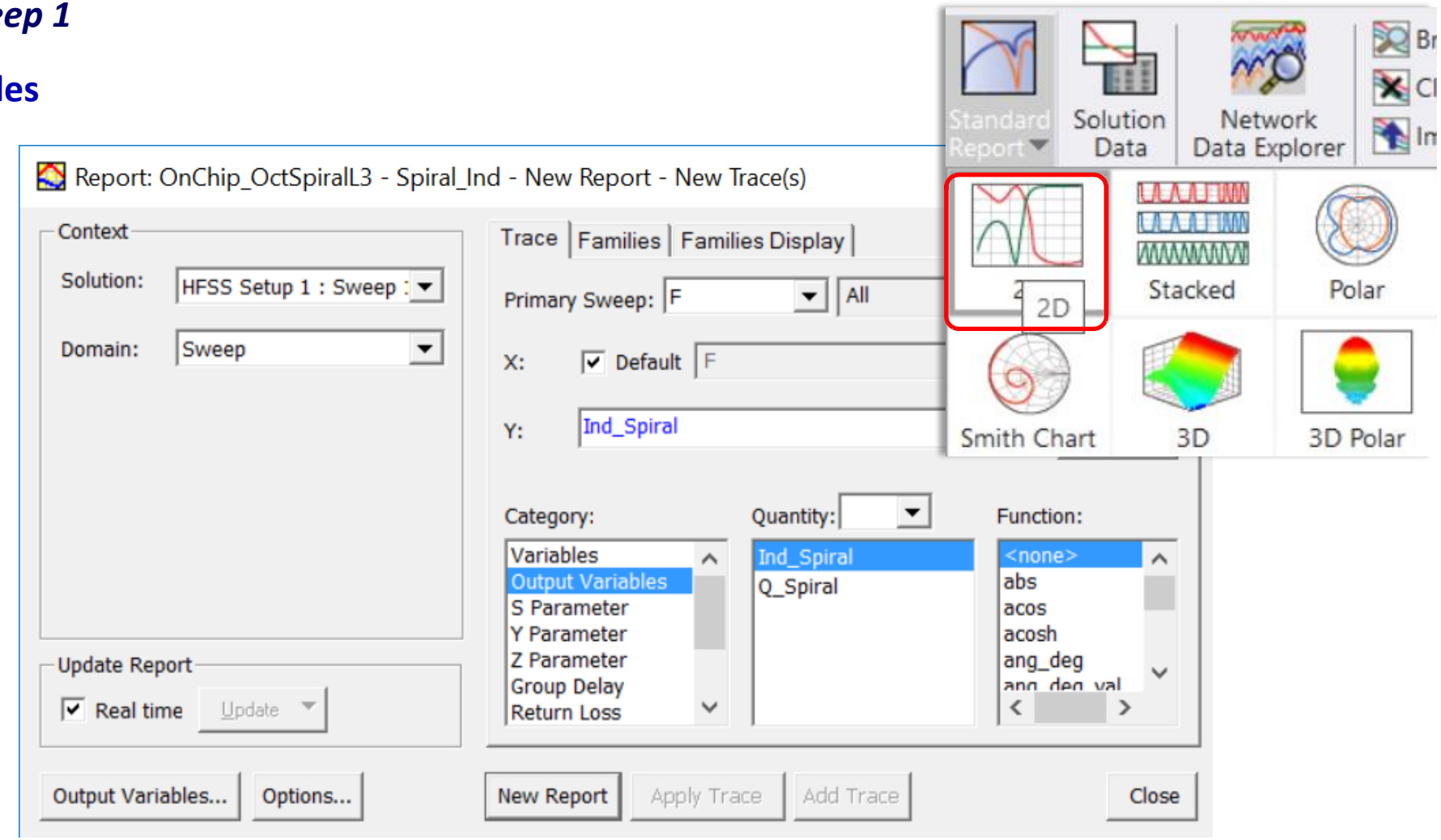




Adaptive passes are performed till both **Mag. Delta S < 0.02** and **Delta for Inductance < 0.05** and **Delta for Q < 0.1**

OnChip_OctSpiralL3.aedt Simulation Results - Inductance Report

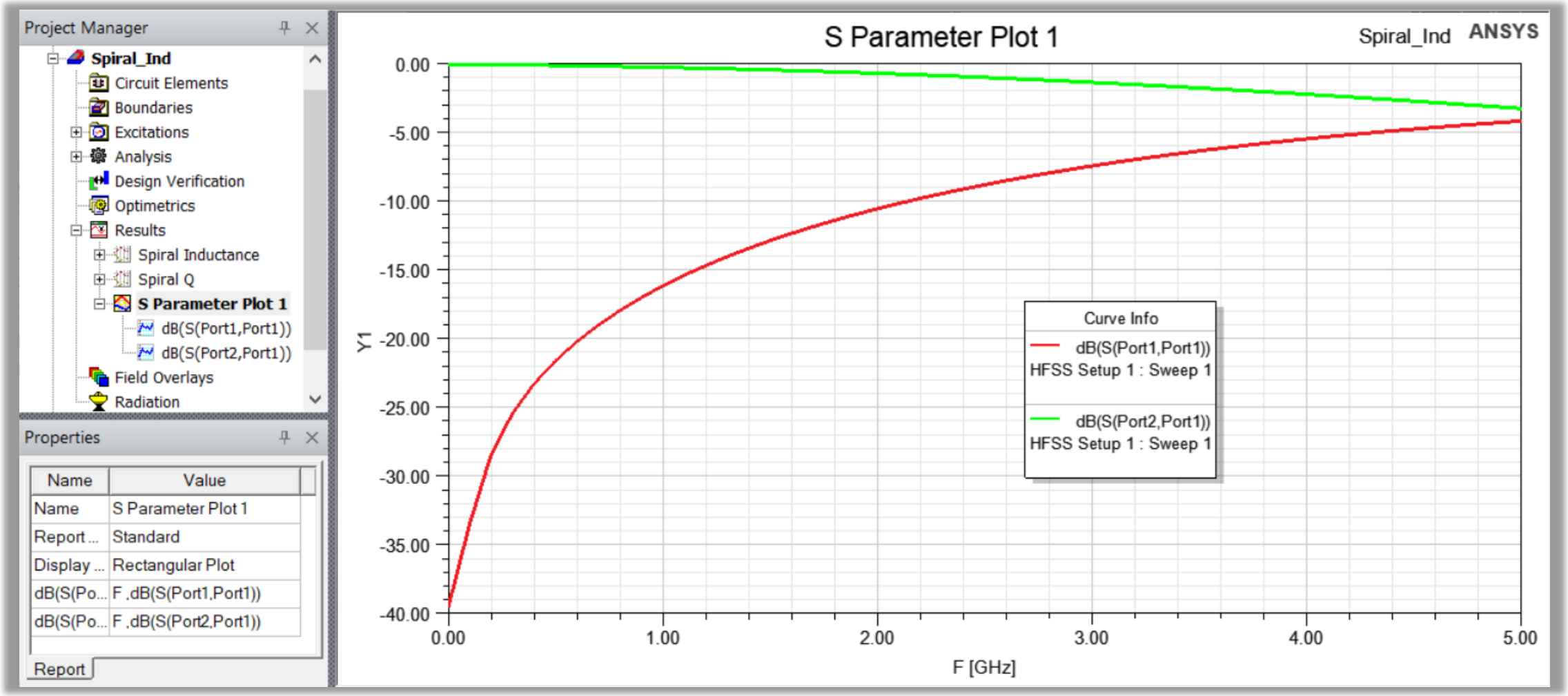
- In the ***Ribbon***, with the **Results** tab selected, click ***Standard Report*** and select ***2D***.
  - Solution: ***HFSS Setup1: Sweep 1***
  - Domain: ***Sweep***
    - ***Category***: **Output Variables**
    - ***Quantity***: **Ind_Spiral**
    - ***Function***: ***<none>***
    - Click ***New Report*** button
  - Click the ***Close*** button



S-Parameters Intuitive Trouble Shooting Check

Post Processing

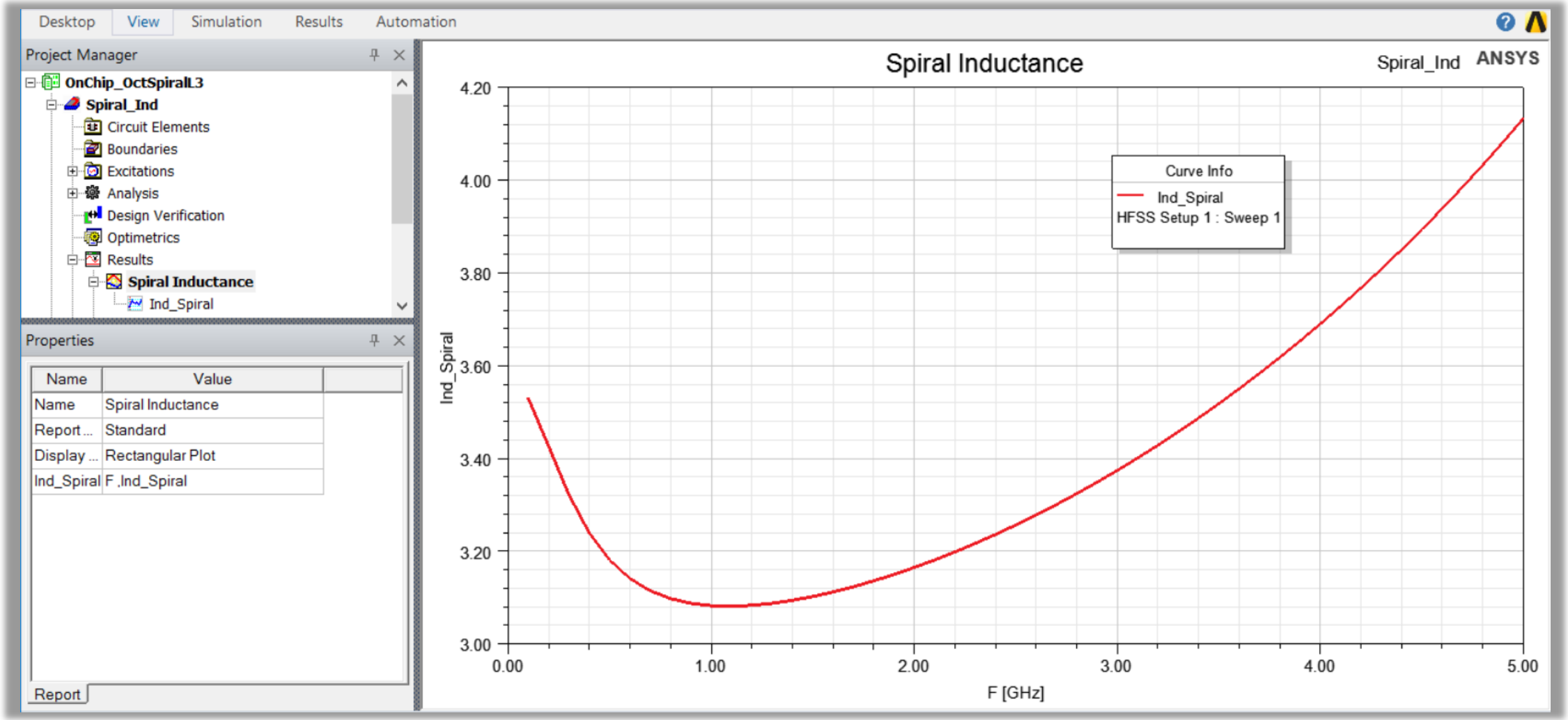
Before looking at the main results for this workshop, the inductance and quality factor, we can do a quick intuitive check using S-parameters. At low frequencies we expect large transmission and small reflection.



Viewing OnChip_OctSpiralL3.aedt Simulation Results: Inductance

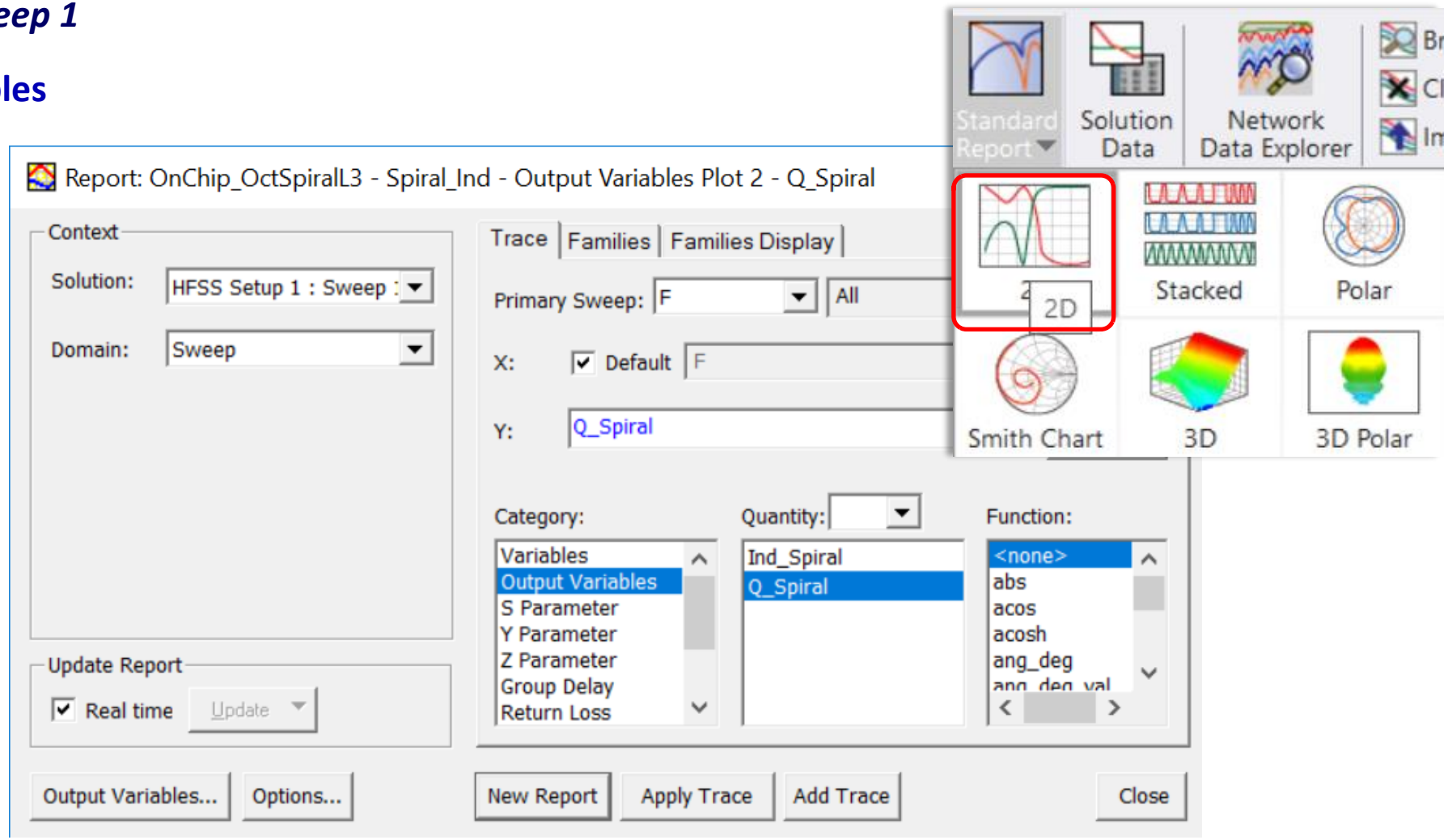
Post Processing

- In the ***Project Manager,*** under ***Results***, right-click on the report and select ***Rename***.
- Change the name of the report to **Spiral Inductance**.



OnChip_OctSpiralL3.aedt Simulation Results - Quality Factor

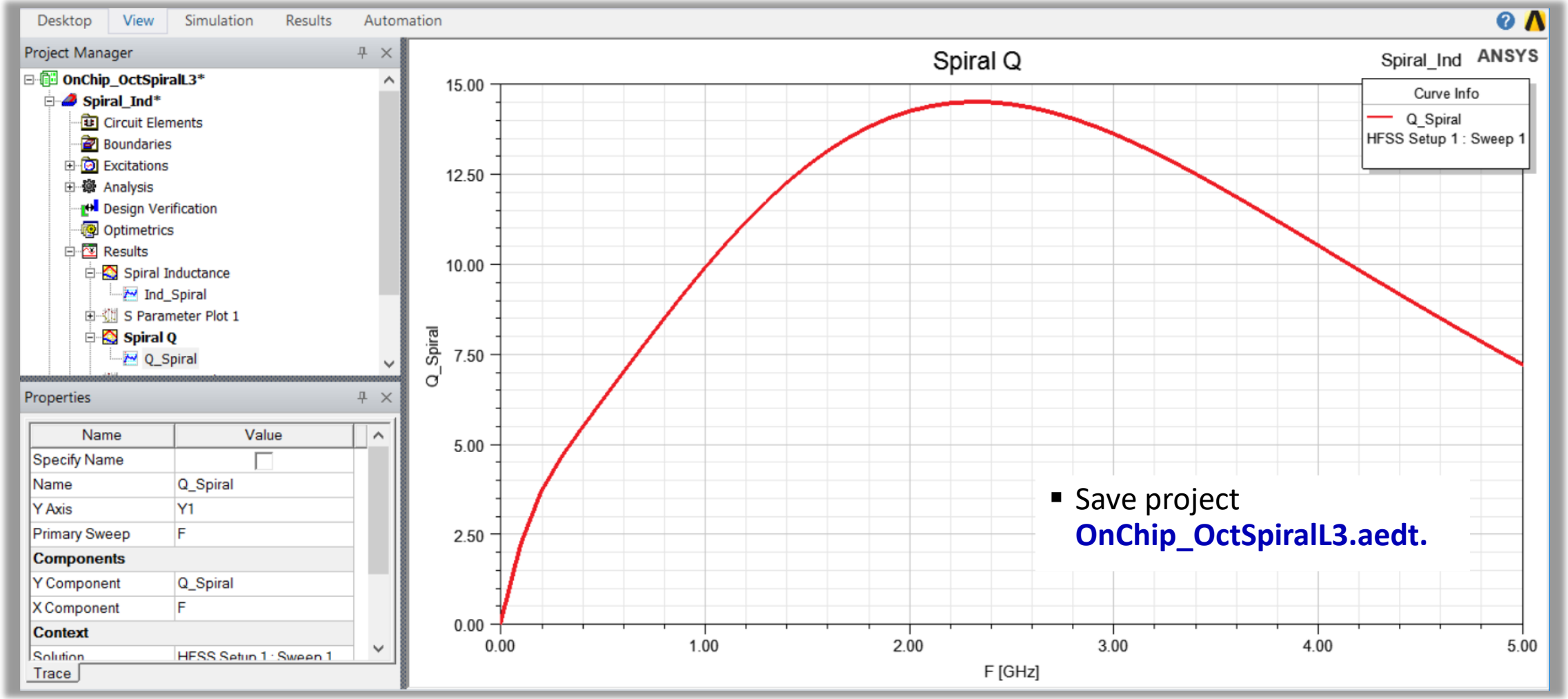
- In the ***Ribbon***, with the **Results** tab selected, click ***Standard Report*** and select ***2D***.
  - Solution: ***HFSS Setup1: Sweep 1***
  - Domain: ***Sweep***
    - ***Category***: **Output Variables**
    - ***Quantity***: **Q_Spiral**
    - ***Function***: ***<none>***
    - Click ***New Report*** button
  - Click the ***Close*** button



Viewing OnChip_OctSpiralL3.aedt Quality Factor Report

Post Processing

- In the ***Project Manager,*** under ***Results***, right-click on the report and select ***Rename***.
- Change the name of the report to **Spiral Q** .



- Save project **OnChip_OctSpiralL3.aedt.**

Solve Options: *Solve Inside* or DC thickness

The default setup for HFSS assumes current flow only on surface of metals. For on-chip applications, circuit dimensions are very small (order of µm). In many cases, for an accurate answer, the skin effect must be modeled and simulated.

HFSS 3D Layout offers two ways to capture skin effect:

1. **Solve inside**

   Enables all the objects in the layer to have "Solve Inside" attribute set for HFSS solver

2. **DC thickness (By default)**

   Controls how DC thickness will be calculated for the conductor lumps on the layers.

- Verify that project **OnChip_OctSpiralL3.aedt** got saved after making reports.

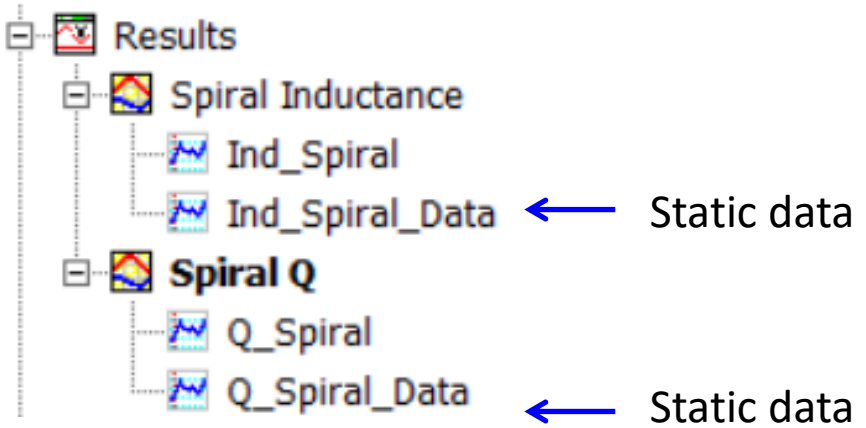
In HFSS online ***Help***, search on skin effect or solve inside. There is one section, titled ***Bulk Conductivity***, that talks about solve inside.

Copy Design to Spiral_Ind_SolveInside - Project OnChip_SpiralL4

Make data copies of existing simulation data

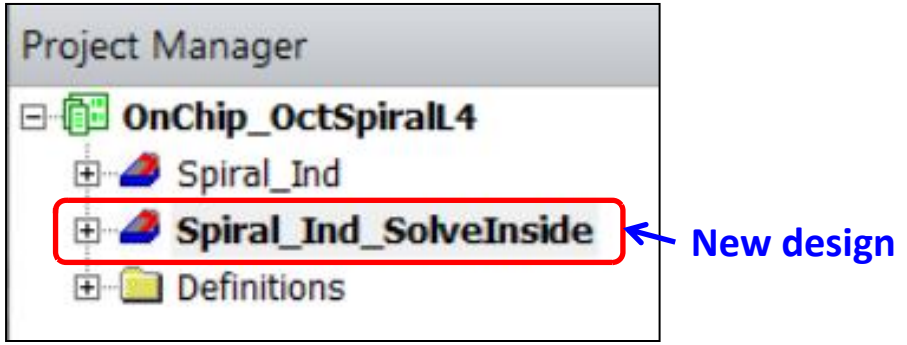
- In the ***Project Manager***, under ***Result***s, under each ***Report***, right-click on the data and select ***Copy Data.***
- Right-click on the ***Report*** name and select ***Paste.***
- Right-click on the new trace and rename it adding the word **Data**.

This copied data won't change when we change the design and resimulate it.



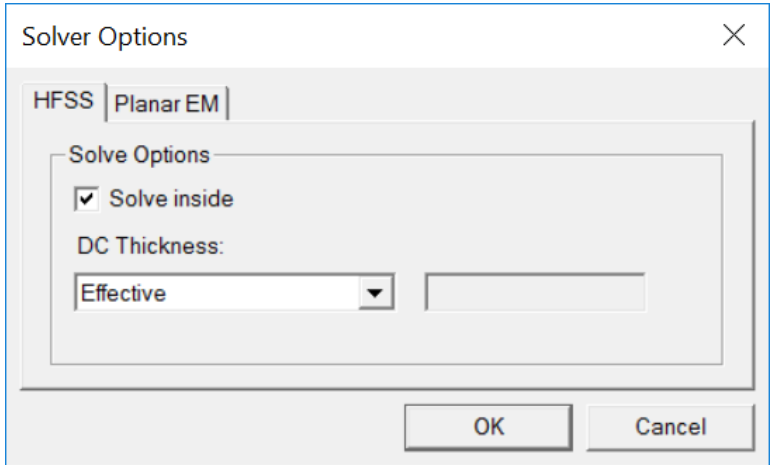
Before modifying the ***Solver Options***, we'll make a copy of the solved design **Spiral_Ind**.

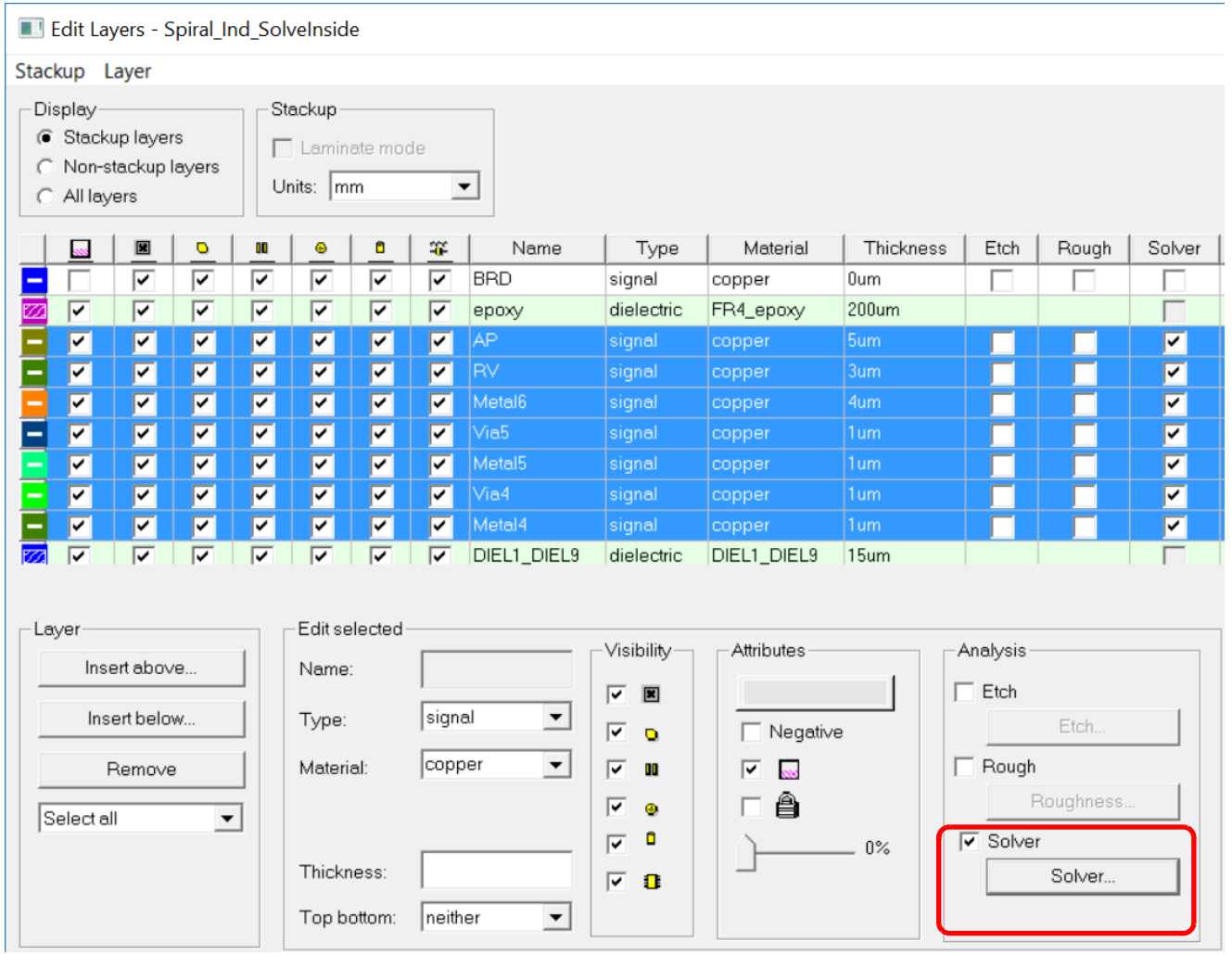
- In the ***Project Manager***, right-click on the design name **Spiral_Ind** and select ***Copy.***
- Right-click on the ***Project*** name ***OnChip_SpiralL3*** and select ***Paste.***
  A new design ***Spiral_Ind1*** will be inserted in the project.
- Right-click on the new design ***Spiral_Ind1*** and select ***Rename.***
- Rename the new design to ***Spiral_Ind_SolveInside***
- Save project to **OnChip_SpiralL4.aedt.**



Set *Solver Options* to *Solve Inside* for Most Copper Layers

- Double-click on the new design ***Spiral_Ind_SolveInside***
- Open the ***Layer Stackup*** window.
  1. Select the layers: ***AP*** through ***Metal4*** using the ***Shift*** key
  2. In the ***Analysis*** area …
     - Check the box for ***Solver***
     - Click the button ***Solver...***
       - Click the ***HFSS*** tab
       - Check the option for ***Solve inside***
       - Click the ***OK*** button
  3. Click the ***Apply and Close*** button





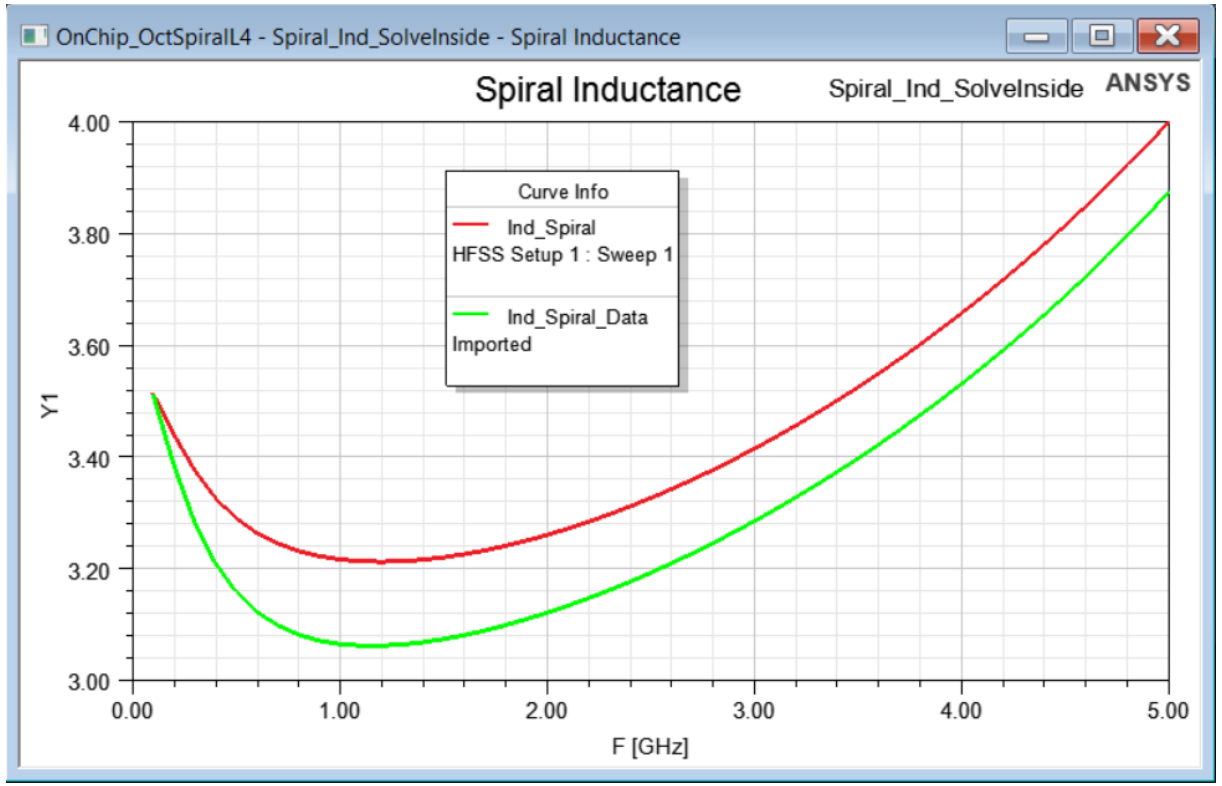
Setting ***Solve Inside*** option overrides the DC Thickness option

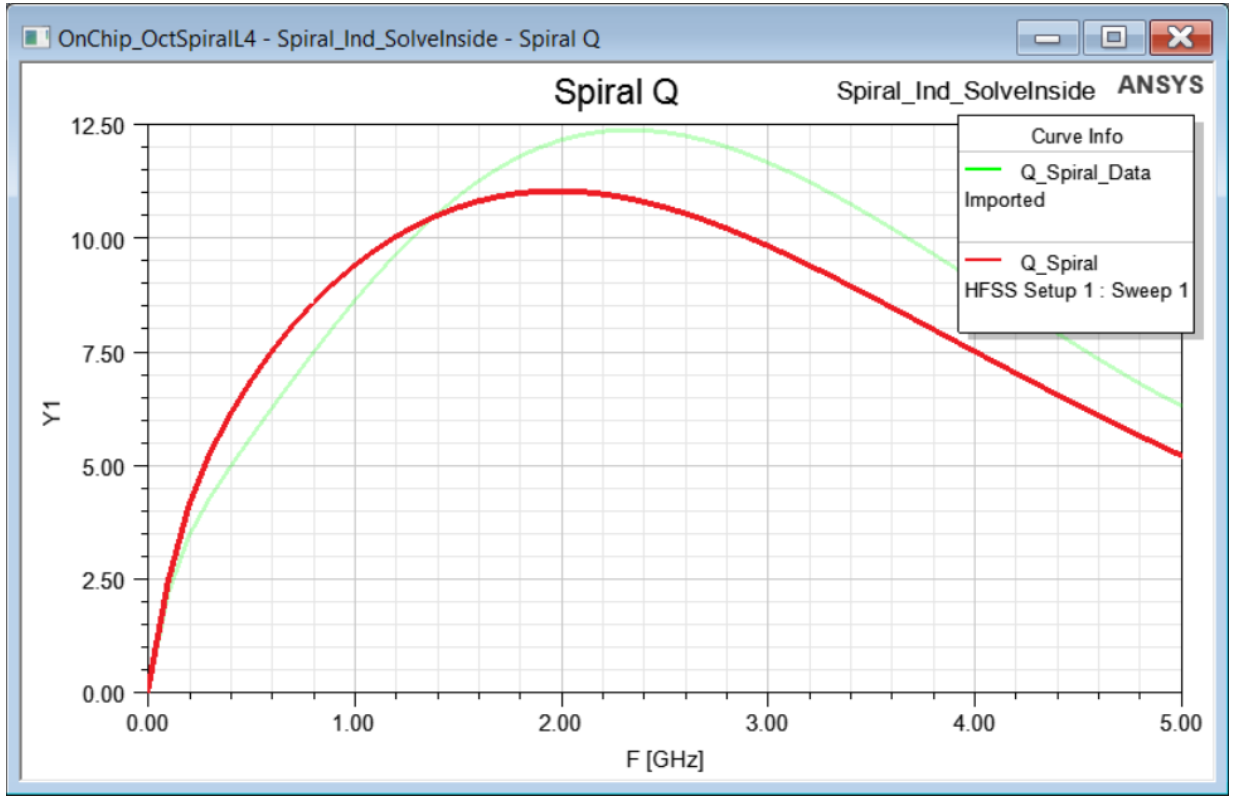
Analyze - Spiral_Ind_SolveInside

- Select the menu item ***HFSS 3D Layout > Analyze***
- In the ***Project Manager***, under ***Results,*** double-click on a plot name.
- ***Imported*** refers to the stored data***.*** The red plots are from ***Solve Inside.***

Simulating ***Solve Inside*** can take significantly more time than the previous simulation.

Inductance/Quality Factor plots using Solve Inside






Ansys