Workshop 6.2: Differential Via TDR

ANSYS HFSS 3D Layout Getting Started Course
WS6.2

Ansys

Outline - Differential Via Time Domain Reflectometry Workshop

HFSS 3D Layout supports circuit simulation hierarchically driving electromagnetic simulation, including transient circuit level simulation for TDR.

1.	Simulate differential via	Diff_CVia1.aedt
2.	Add circuit to project and add hierarchy	Diff_CVia_TDR1.aedt
3.	Add circuit elements	Diff_CVia_TDR1.aedt
4.	Add grounds and TDR specifications	Diff_CVia_TDR2.aedt
5.	Add TDR Nexxim simulation setup and analyze	Diff_CVia_TDR3.aedt
6.	Select stripline traces and move to different layer	Diff_CVia_TDR5.aedt
7.	Adjust padstack to remove via stubs	Diff_CVia_TDR6.aedt
8.	Remove via stubs and resimulate	Diff_CVia_TDR4.aedt

Case 1: long via - stripline on low layer

Case 2: stripline moved up - via stub remains

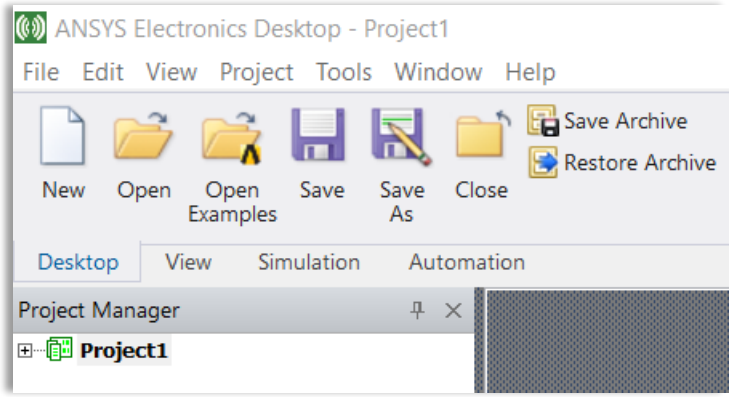
Case 3: via stub removed in padstack usage

HFSS: Launching ANSYS Electronics Desktop

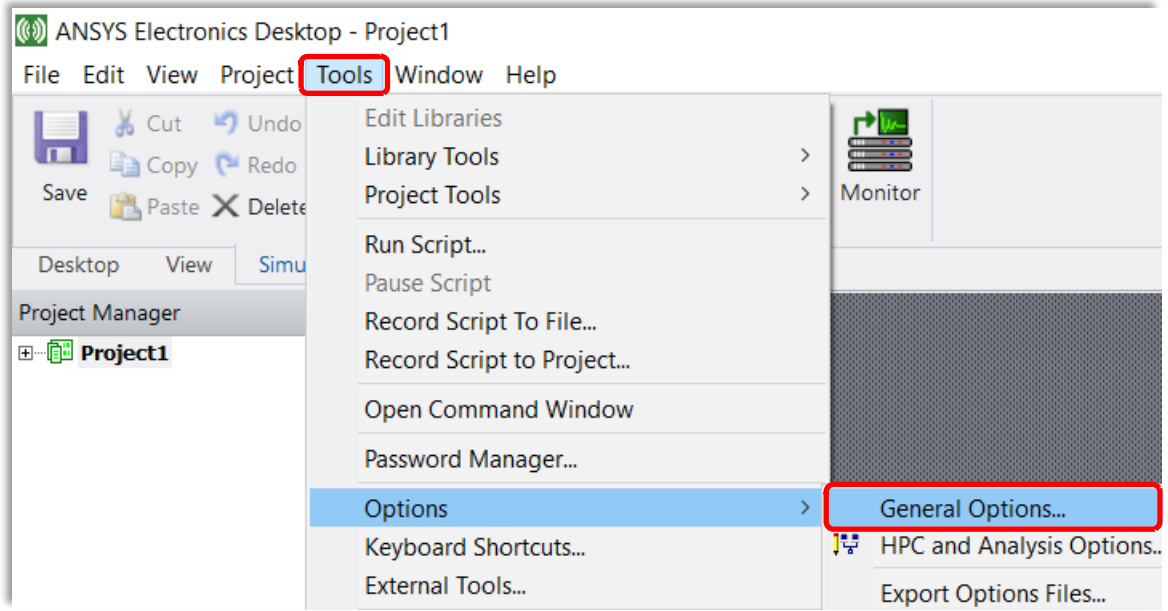
Open HFSS and Set Options (if not already set)

- To access HFSS, click the Microsoft Start button, Select:
  Programs > ANSYS Electromagnetic Suite > ANSYS Electronics Desktop

  A new "Project1" appears under the Project Manager.
- Setting Tool Options ***(skip this slide and two more if already done.)***
  Select the menu item ***Tools > Options > General Options***



Option settings suggested here ensure that the user can consistently follow the steps in the Workshop.

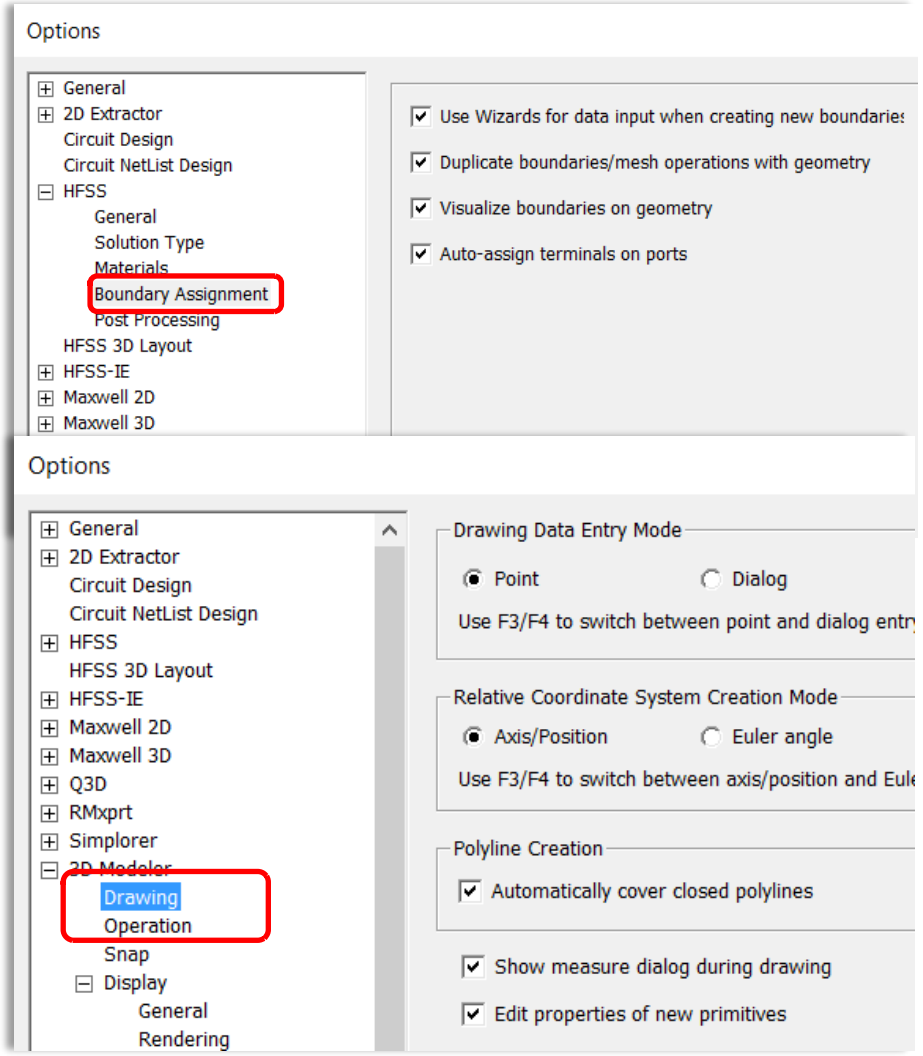


Setting *Tool > Options* for HFSS 1 - Boundary, Drawing, and mm

- Selected: ***Tools > Options > General Options***
- Expand ***General*** (by clicking on the + sign) and Select ***Default Units***
  - Set Length to ***mm***
- Expand ***HFSS*** (by clicking on the + sign) and Select ***Boundary Assignment***
  - ***Check all entries***
- Expand ***3D Modeler*** and click ***Drawing***
  - **Automatically cover closed polylines: ☑ Checked**
  - **Edit properties of new primitives: ☑ Checked**

…continued…

Option settings suggested here ensure that the user can consistently follow the steps in the Workshop.

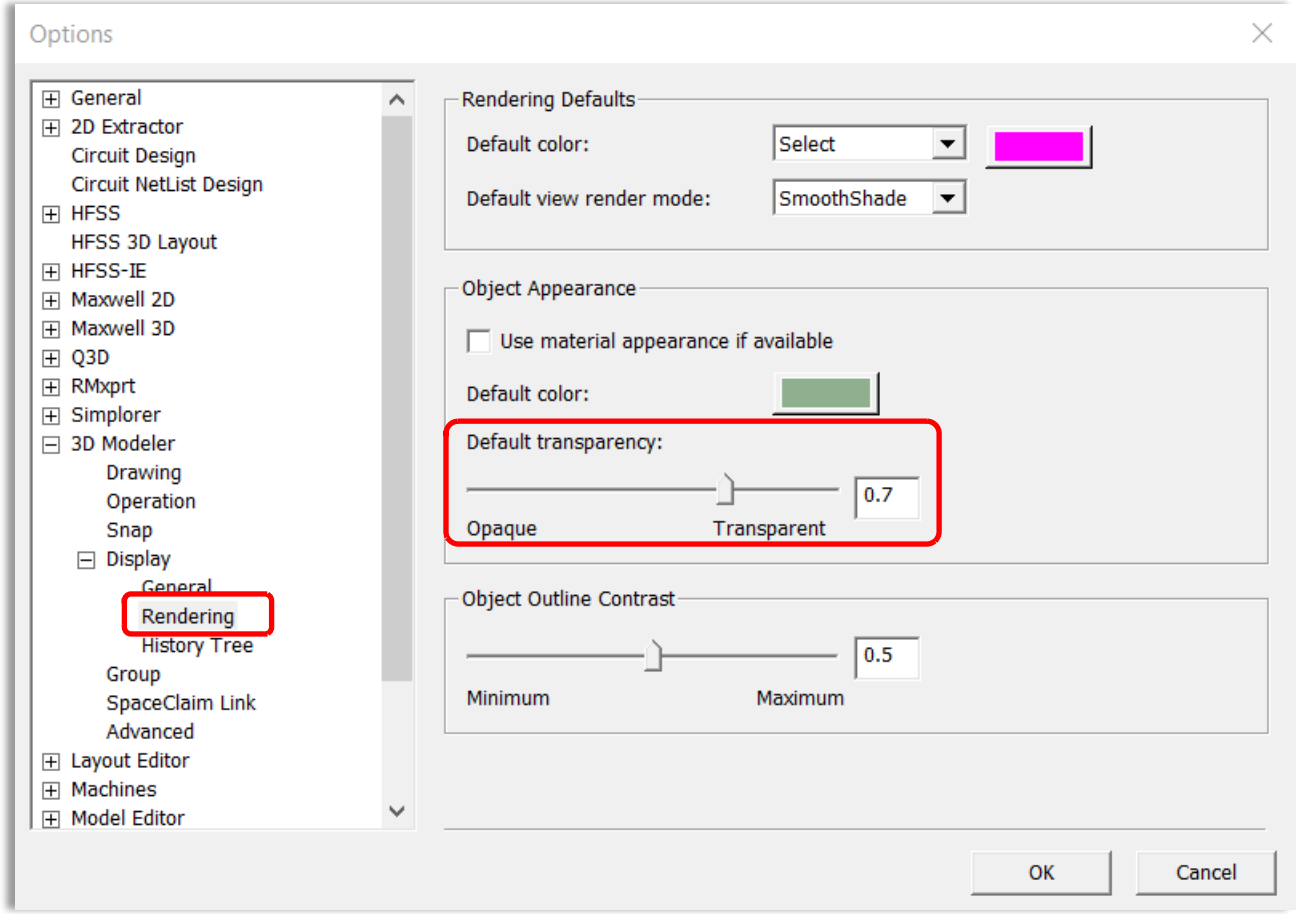


Setting *Tool > Options* for HFSS 2 - Display History and Transparency

- Expand ***Display***
  - Click ***Rendering*** and set ***Default Transparency*** to **0.7**
  - Click ***History Tree*** and ***check all entries*** (not shown here)

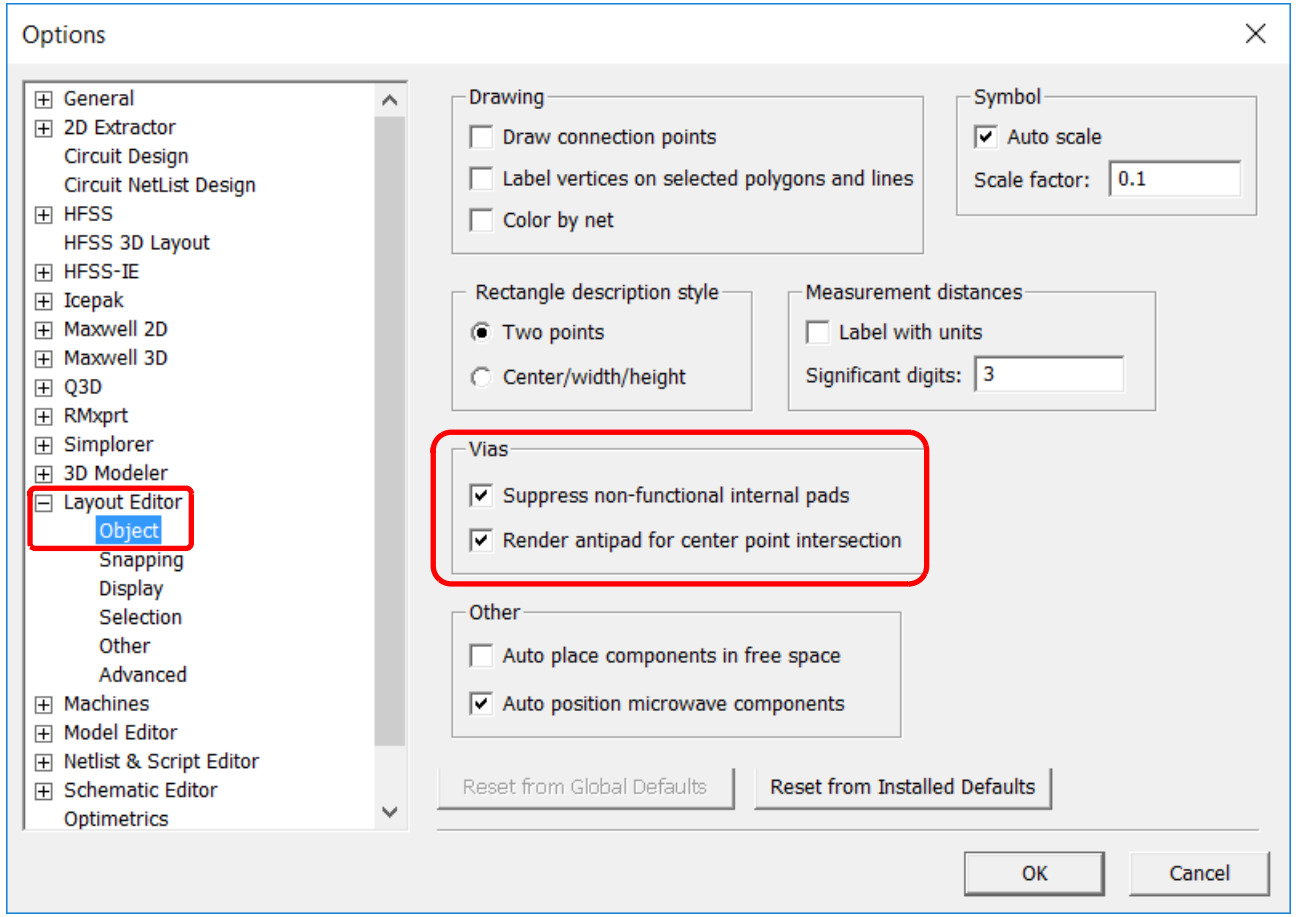
…continued…

Option settings suggested here ensure that the user can consistently follow the steps in the Workshop.



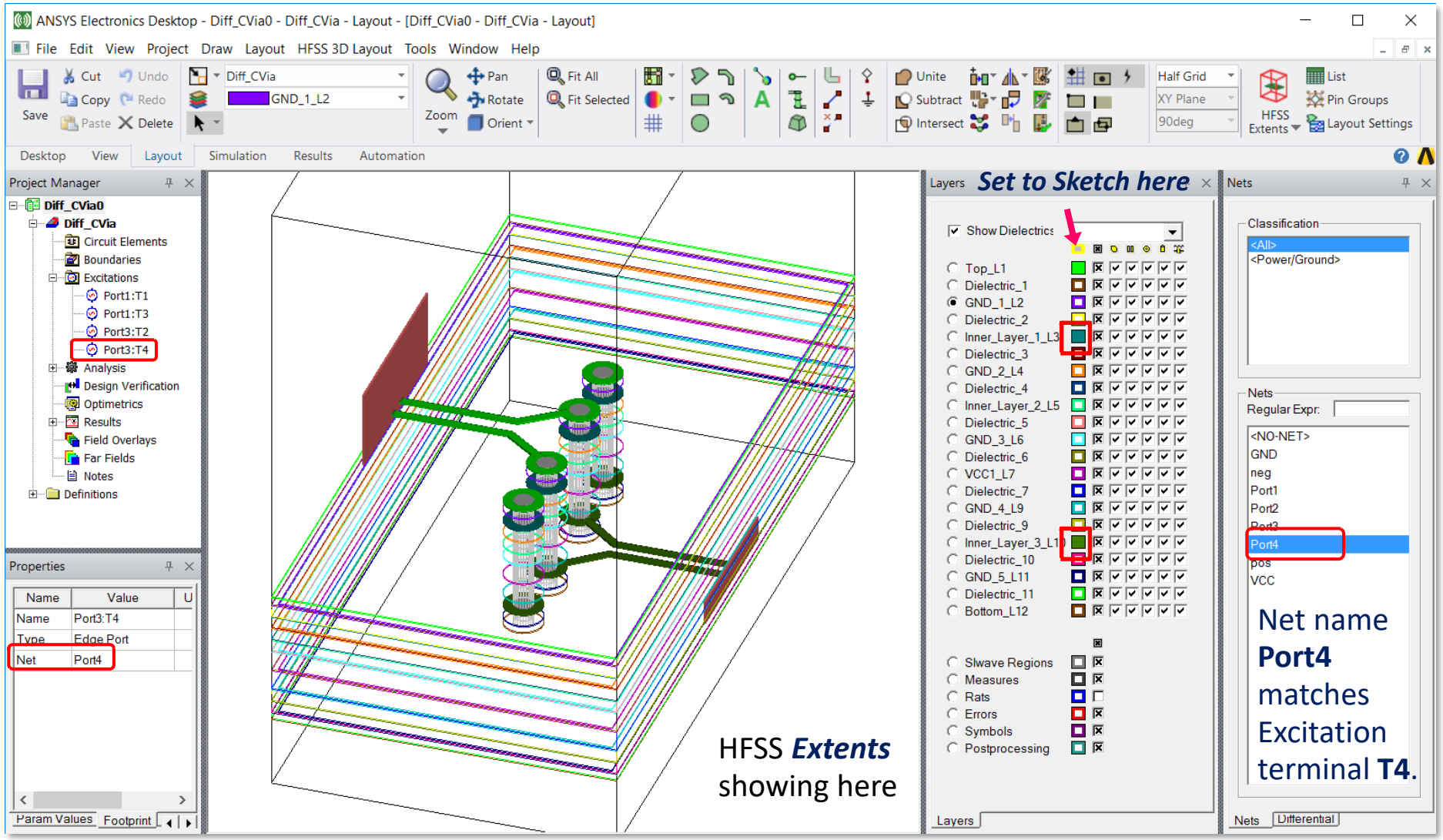
Setting *Tool > Options* for HFSS 3 - Internal Pads - Diff_CVia0.aedt

- Expand ***Layout Editor***
  - Verify that both selections under ***Vias*** are checked.
- Click the ***OK*** button to close ***Options*** dialog box.
- Select ***File > Open***… and browse to the provided training files.
- Open **Diff_CVia.aedt**.
- Save to a working directory as **Diff_CVia0.aedt**.

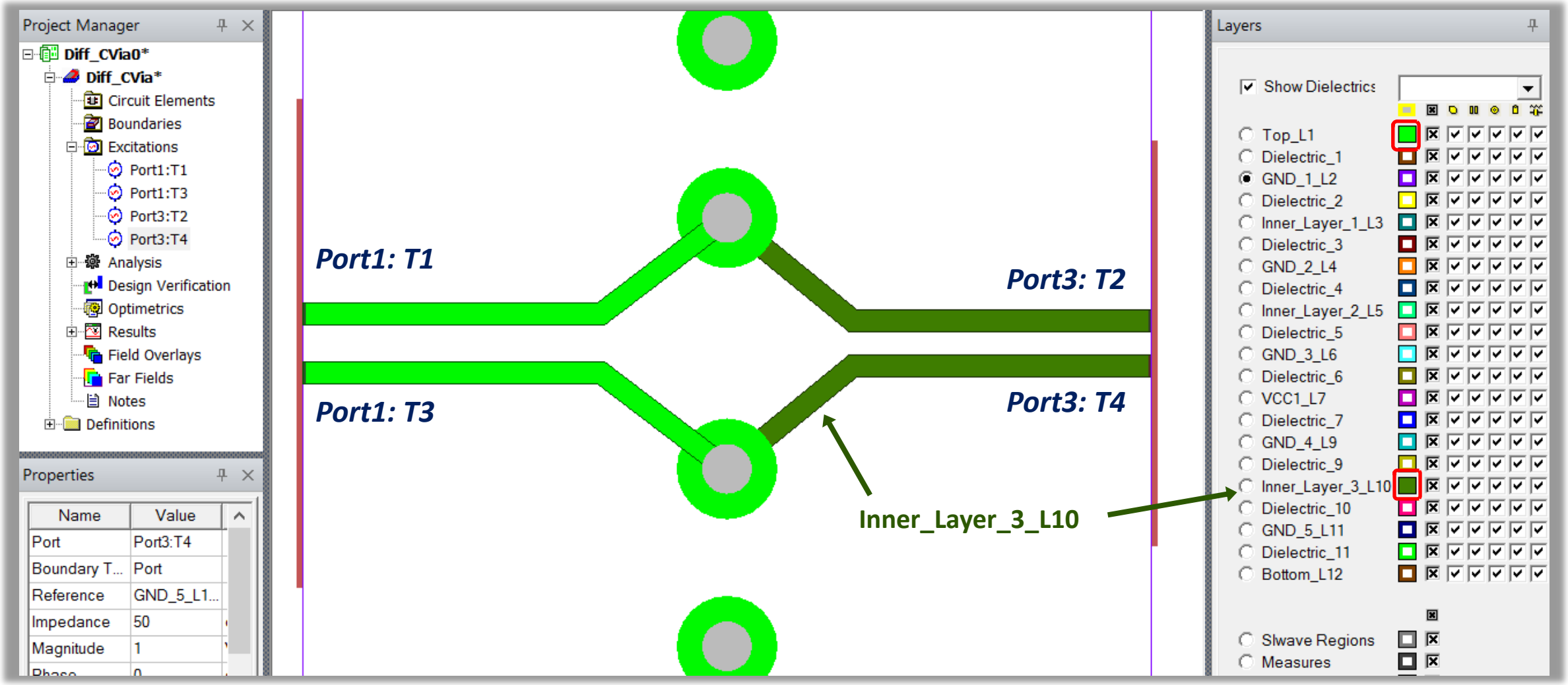


Option settings suggested here ensure that the user can consistently follow the steps in the Workshop.

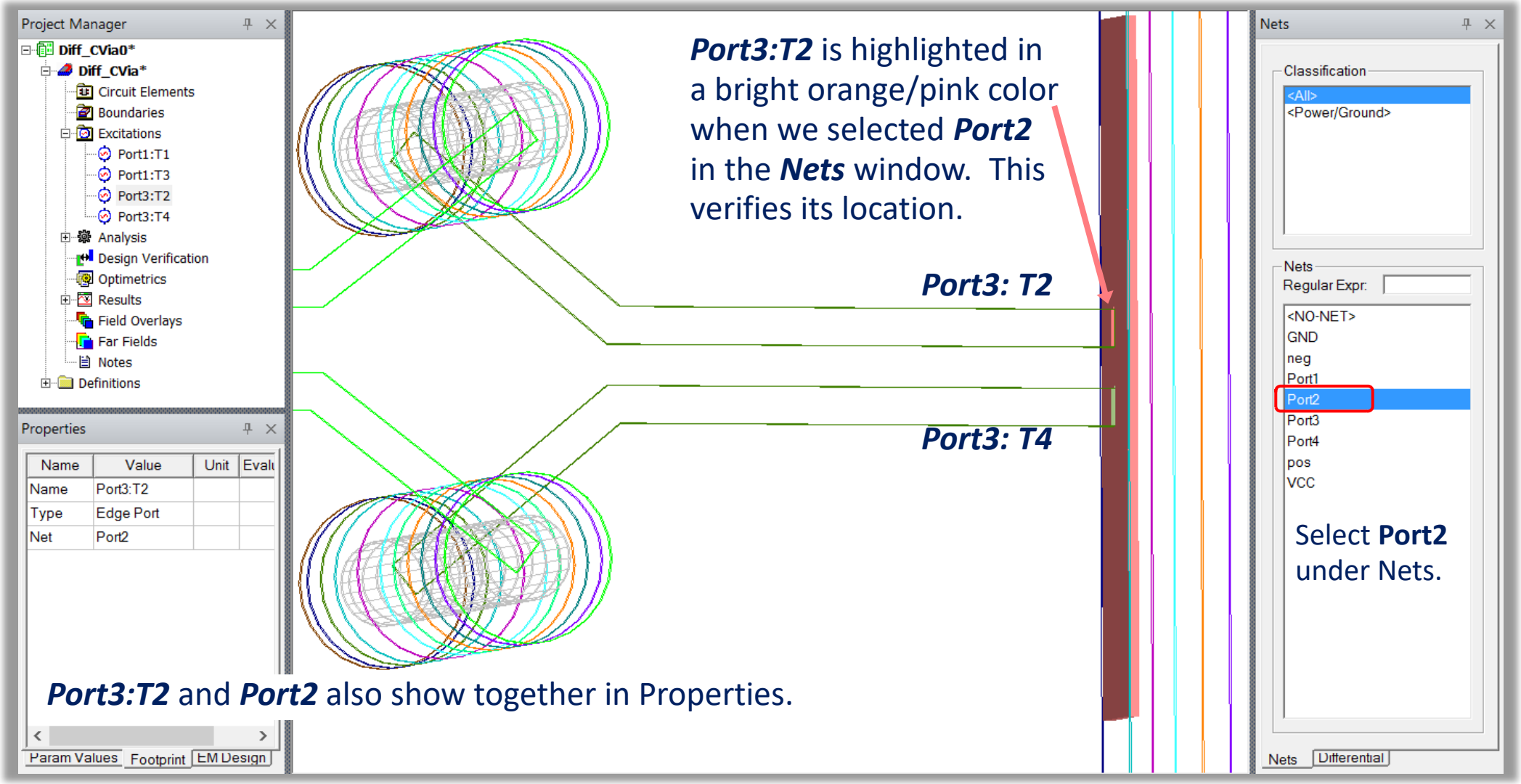
Starting Project Diff_CVia0.aedt - Showing Extents and Nets



Starting Project Diff_CVia0.aedt - Terminals Aligned for S-params



Diff_CVia0.aedt - Verifying Terminal Locations



Verify Project Diff_CVia0.aedt *Cosim Options*

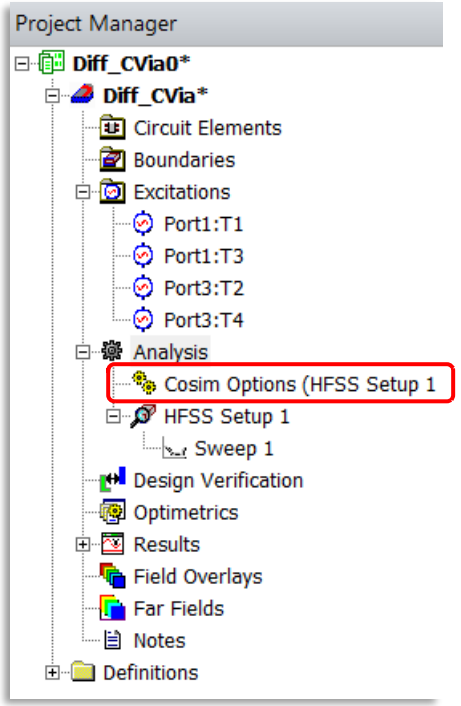
- In the ***Project Manager***, under ***Analysis***, double-click on ***Cosim Options*** to bring up the ***Co-Simulation Options*** dialog box.
- Verify ***Cosim Options***

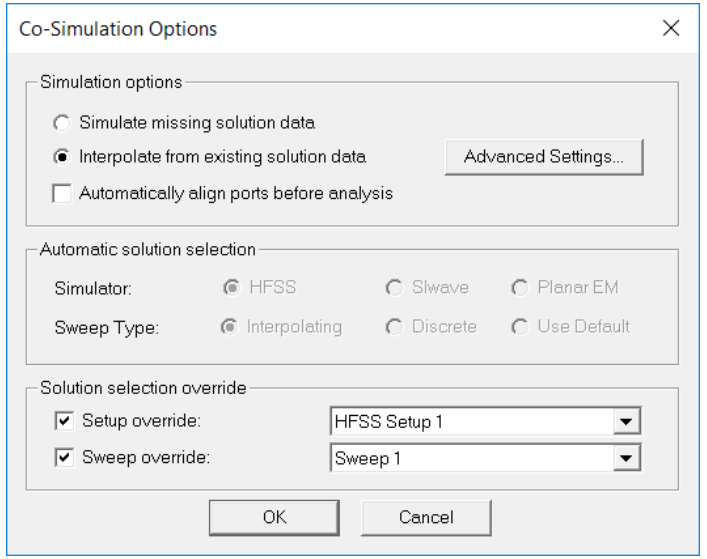
  Interpolate from existing solution data ☑ checked

  Solution selection override ☑ checked

  Setup override ☑ checked and set to ***HFSS Setup 1.***

  Sweep override ☑ checked and set to ***Sweep 1***.
- Click on ***OK*** to close the ***Co-Simulation Options*** dialog box.





Verify Project Diff_CVia0.aedt *Solution Setup Options*

- In the ***Project Manager***, under ***Analysis***, double-click on ***HFSS Setup 1*** to bring up the ***HFSS Setup 1*** dialog box.
- Verify ***HFSS Solution Setup*** (***HFSS Setup 1***)

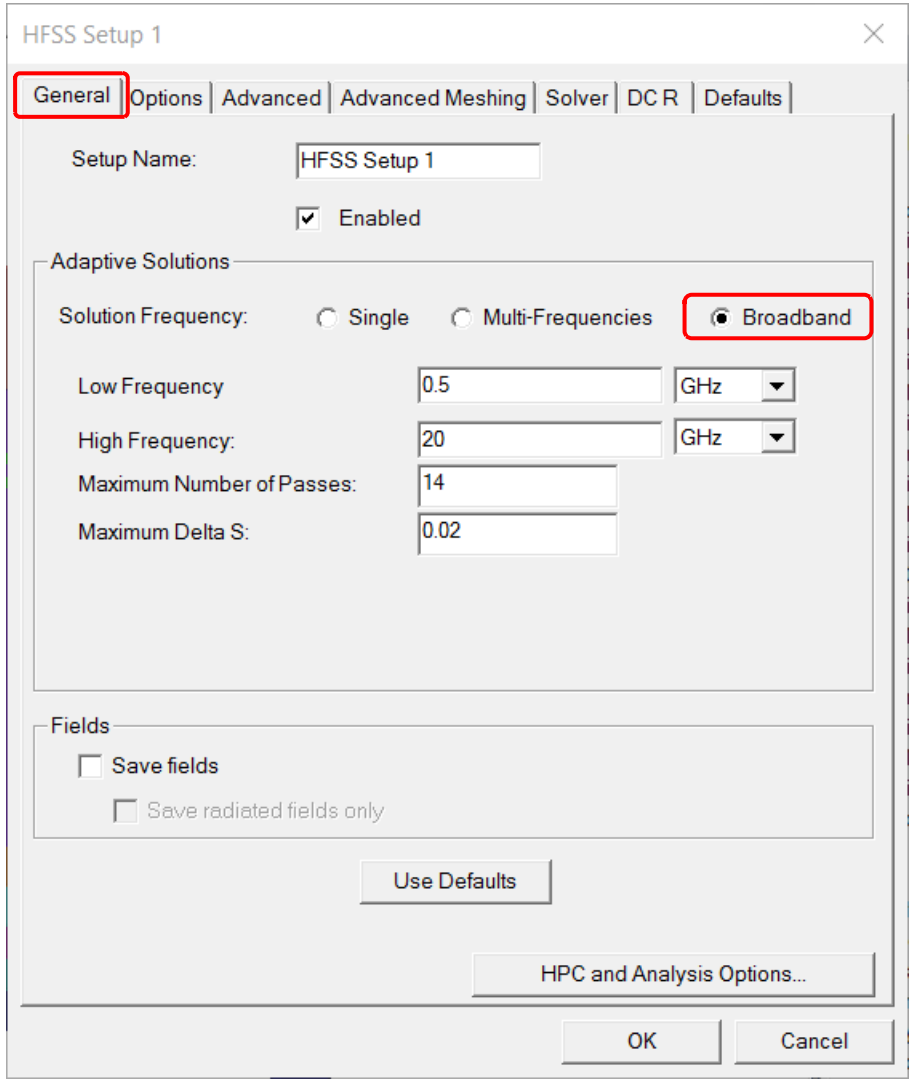
  Solution Frequency: **Broadband**

  Low Frequency **0.5 GHz**

  High Frequency **20 GHz**

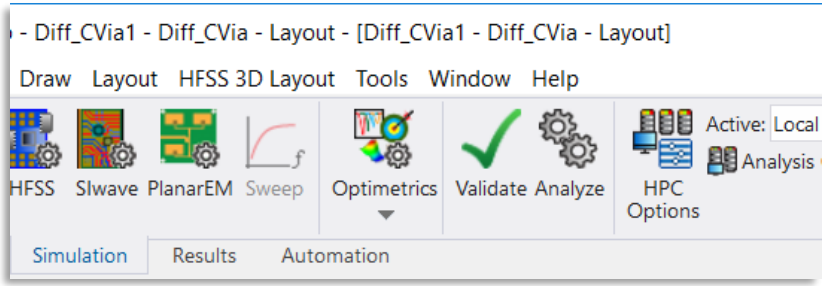
  Maximum Number of Passes **14**

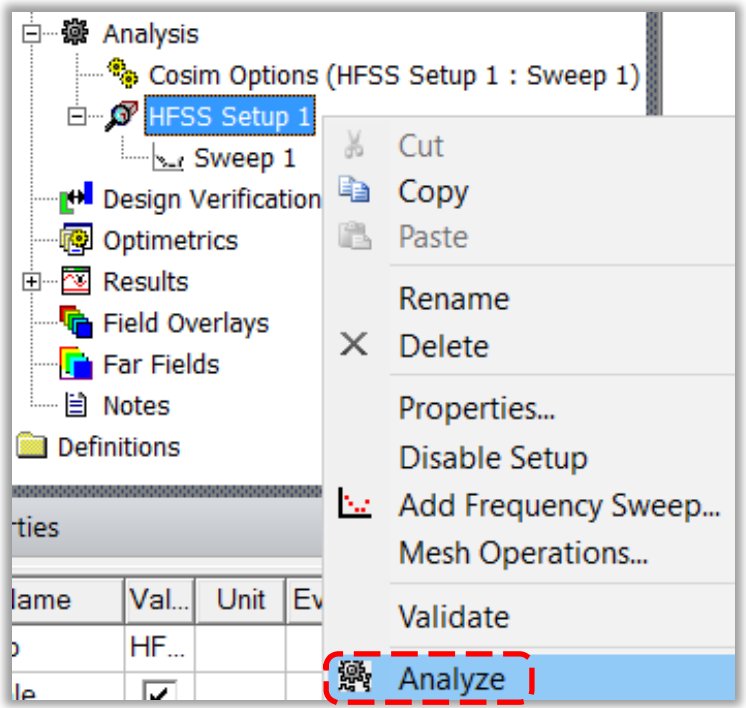
  Maximum Delta S **0.02**
- Click on ***OK*** to close the ***Co-Simulation Options*** dialog box.
- Save file to **Diff_CVia1.aedt**

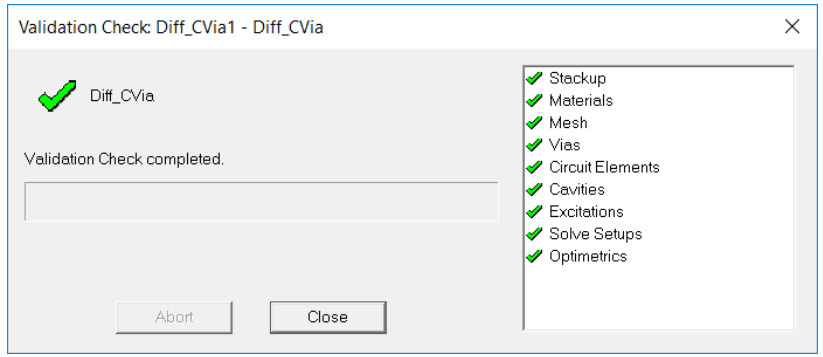


Validate and Analyze Diff_CVia1.aedt

- If not done already, ***Save As* Diff_CVia1.aedt.**
- In the ribbon, with the **Simulation** tab selected, click on ***Validate*.**
- In the ***Project Manager***, under ***Analysis,*** right-click on ***HFSS Setup 1*** and select ***Analyze*.**
- When simulation is finished ***Save*** project **Diff_CVia1.aedt** again.



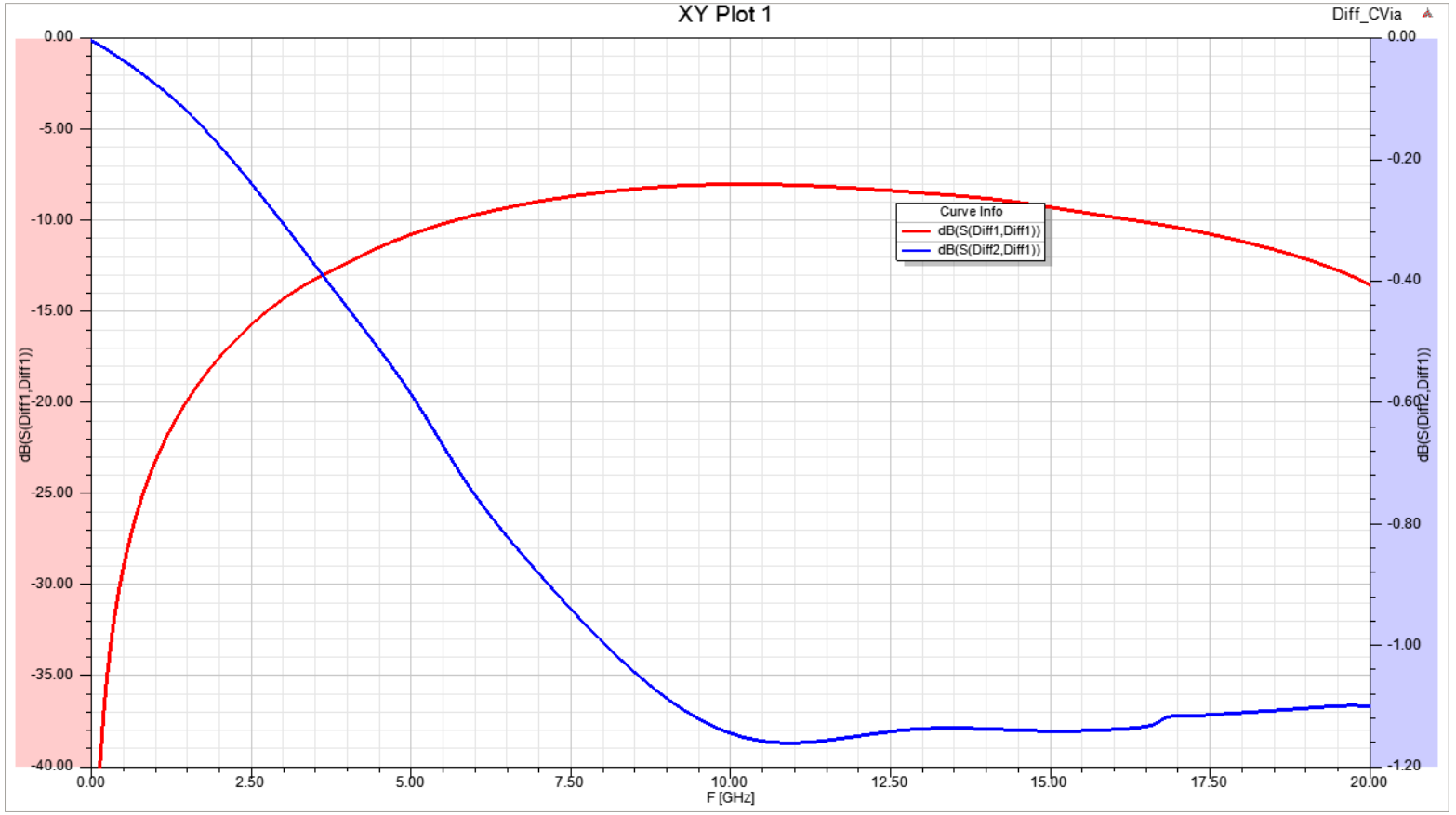




Diff_CVia1.aedt Simulation Results

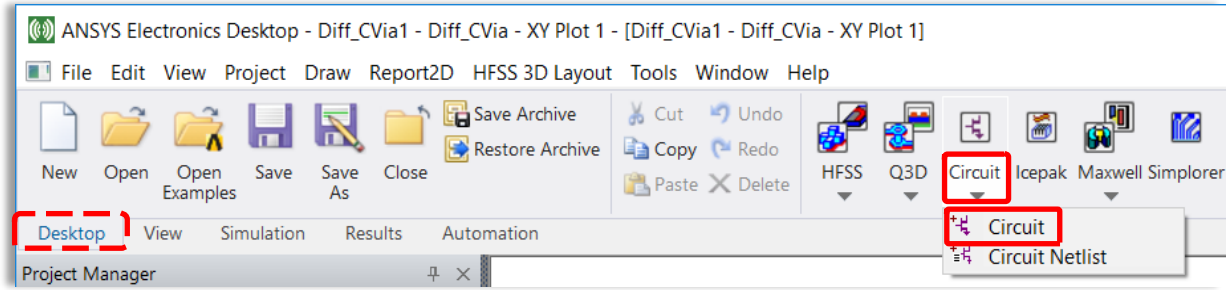
The reflection term, on the left hand scale, gets as high as about -8 dB at 10 GHz.

The transmission term, on the right hand scale, gets below -1 dB just above 7.5 GHz.

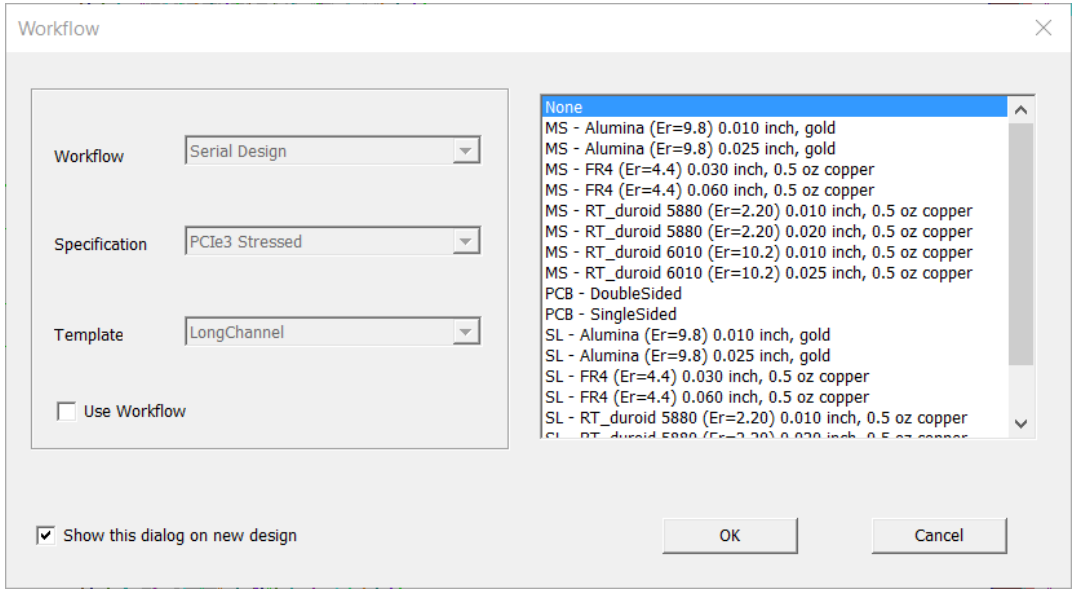


Add a *Circuit* Design to the Project Diff_CVia1.aedt

- In the ***Project Manager***, double-click on the design name **Diff_Cvia** to get the design view showing on screen.



- In the **Ribbon**, with the **Desktop** tab highlighted, click on the triangle below ***Circuit*** and select ***Circuit*** to insert a circuit design into the project. This action brings up the ***Workflow*** dialog box.
- In the ***Workflow*** dialog box select ***None***.
- Click ***OK*** to close the ***Workflow*** dialog box.



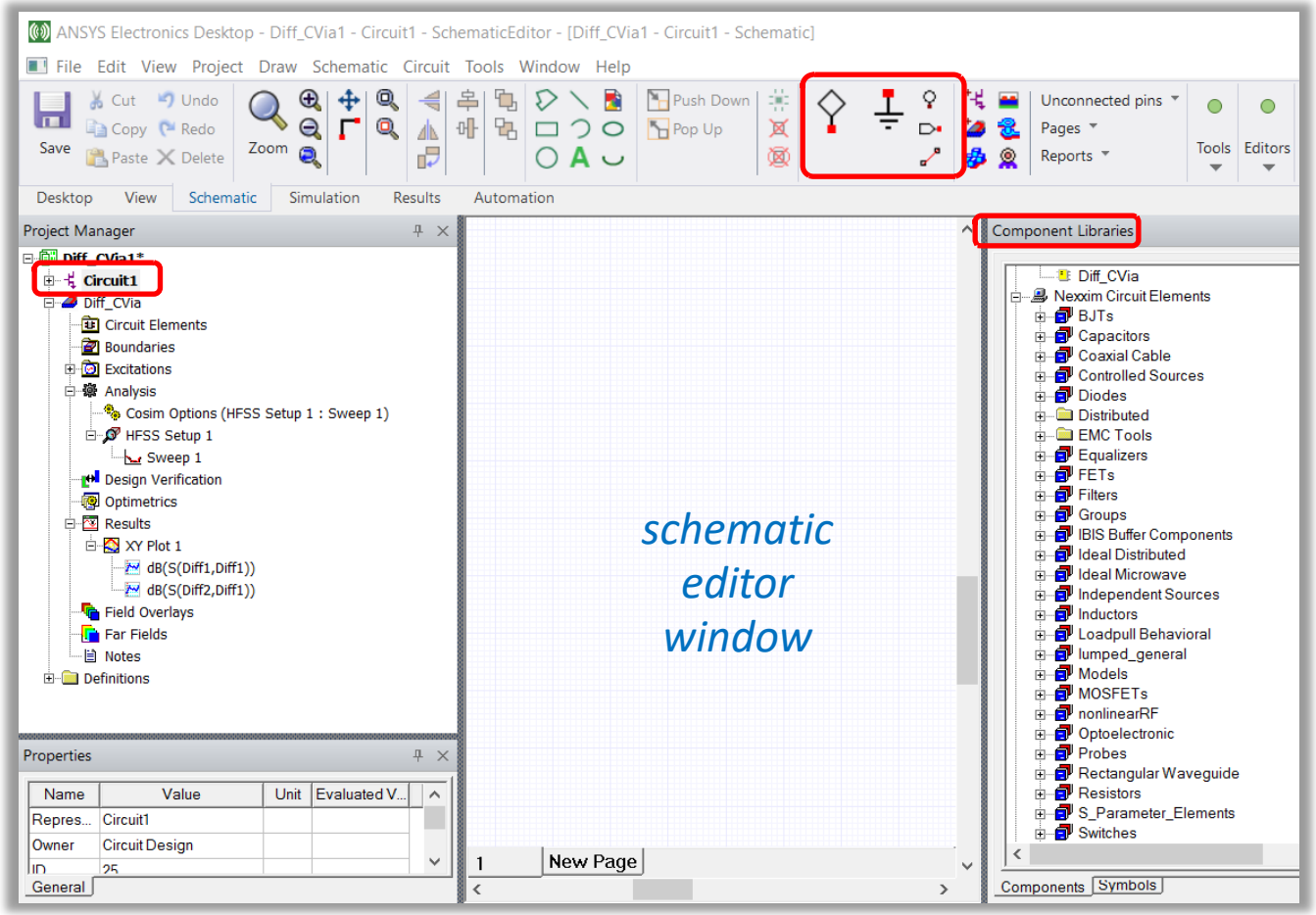
New *Circuit* Design in the *Project Manager*

After inserting a circuit design into the project, we see a circuit design **Circuit1** in the ***Project Manager***.

There is a ***Component Library*** menu and the **schematic editor** window appears.

Also notice the tools and symbols available in the Ribbon **Schematic** tab.

Now there is a circuit design and an HFSS 3D Layout design at the same level of hierarchy within the project. Next we'll place the HFSS layout underneath the circuit.

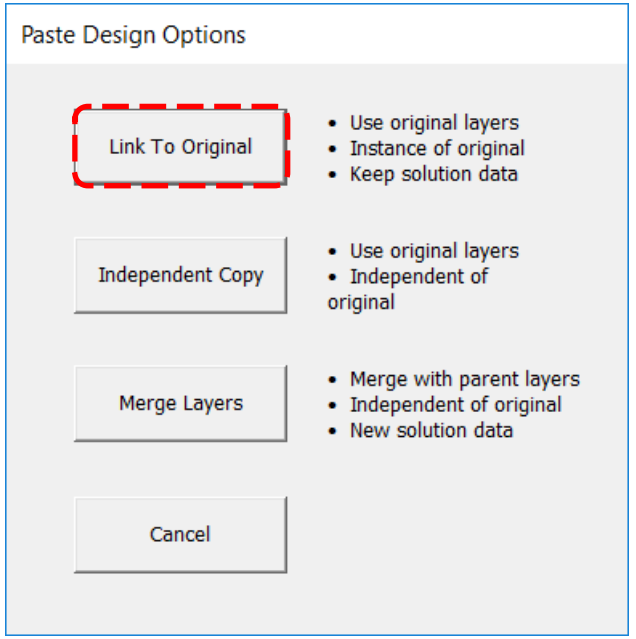


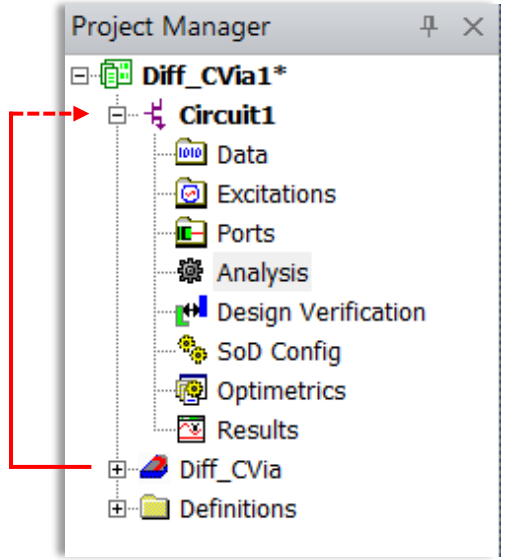
Move the Via Design into the Circuit

- In the ***Project Manager***, left-click and drag the HFSS ECAD layout design **Diff_CVia** to the circuit design **EyeCircuit**.

- This brings up the ***Paste Design Options*** menu on screen.
- Click on ***Link to Original***.

This step creates hierarchy. Now the differential via EM model becomes a circuit element on the schematic.





The Via Design Hierarchy Under the Circuit - Diff_CVia_Eye1.aedt

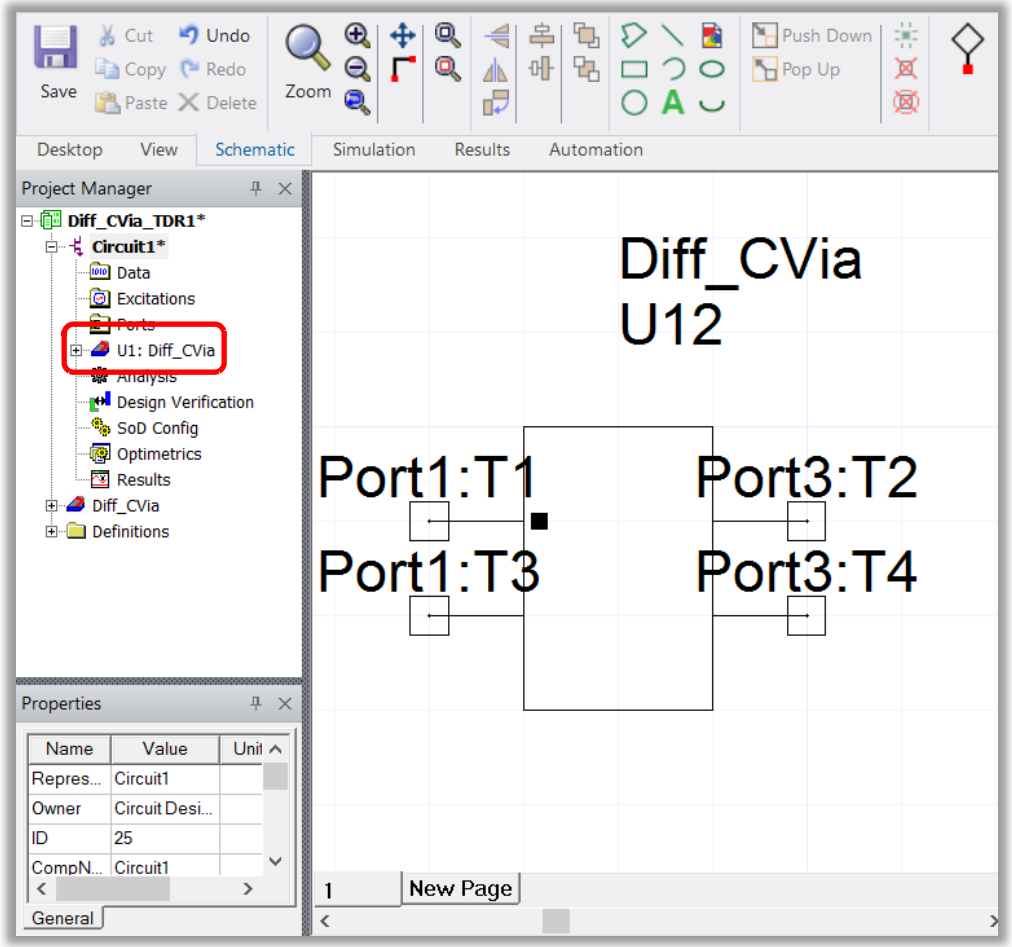
After copying the HFSS 3D Layout via design into the circuit, we see the via schematic symbol on the schematic.

The HFSS 3D Layout via design **U1: Diff_CVia** is now hierarchically within **EyeCircuit.**

The original independent HFSS 3D Layout via design **Diff_CVia** is also still in the project and the two differential via models are linked.

The U number on the schematic increments separately from the **U1** in the ***Project Manager.*** ***(Ctrl-D*** was used to increase the size of the symbol in the schematic view.)

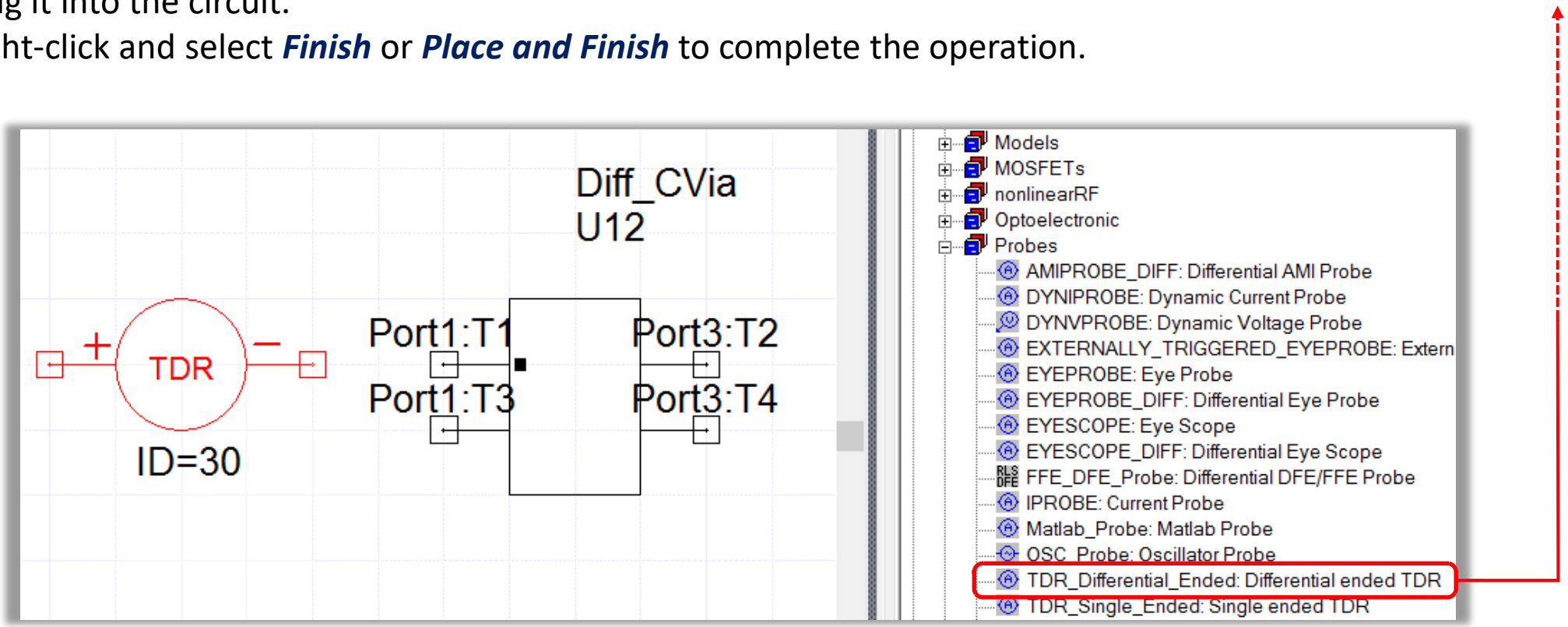
- Save the project to **Diff_CVia_Eye1.aedt**.



schematic editor window

Add TDR Probe to the Circuit - Diff_CVia_TDR1.aedt

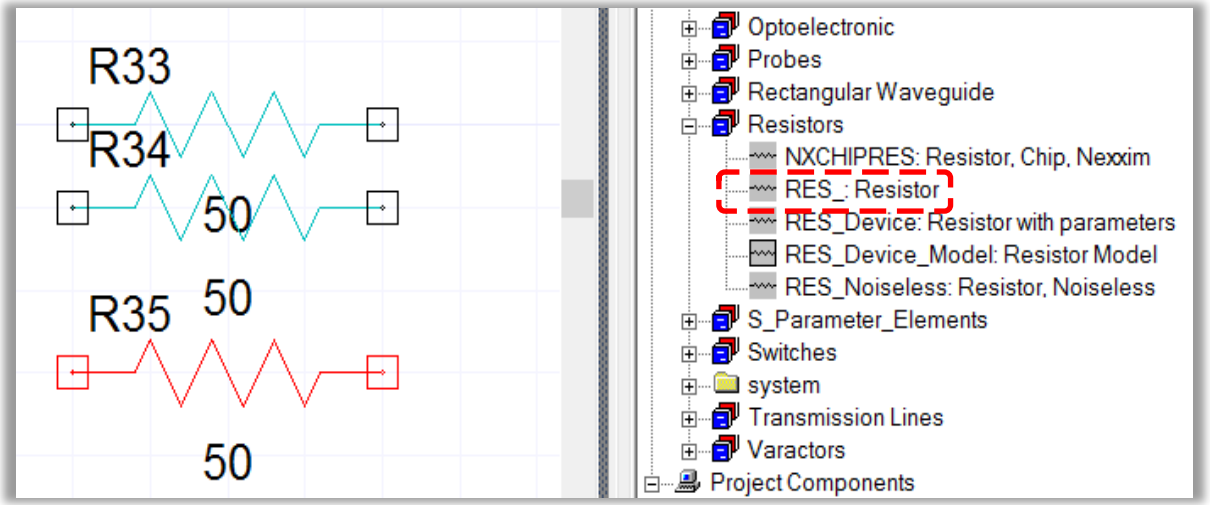
- From the ***Component Libraries*** menu, under ***Nexxim Circuit Elements***, under ***Probes***, select a differential TDR and drag it into the circuit.
- Right-click and select ***Finish*** or ***Place and Finish*** to complete the operation.

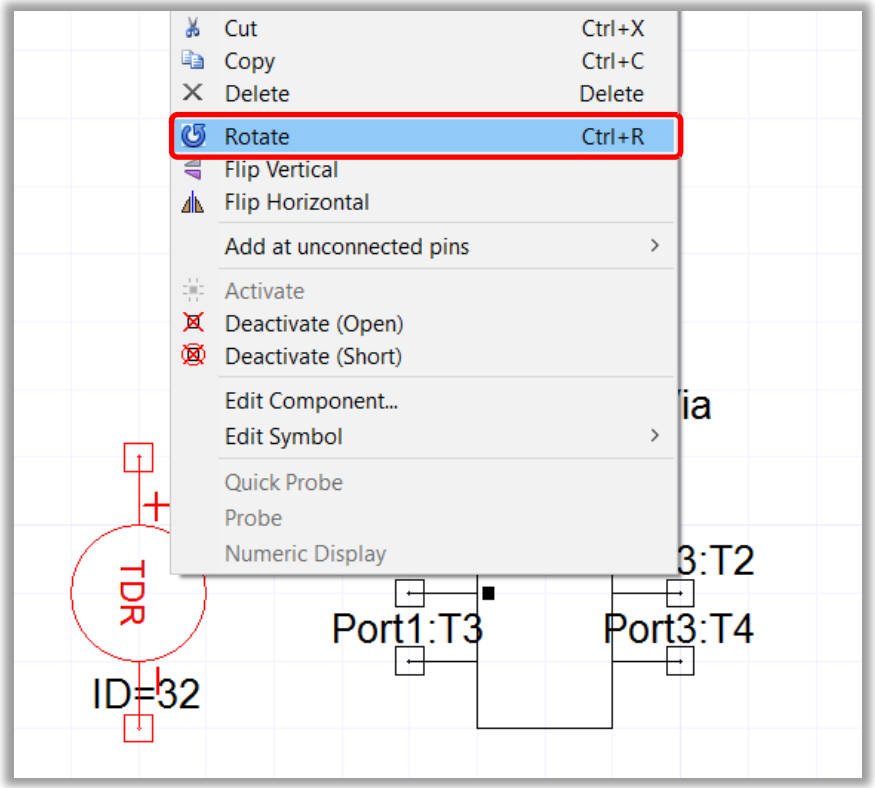


*Components can be rotated before placement by clicking on the **R** key.*

Rotate TDR Probe and Add Resistors to the Schematic

- Right-click on the TDR probe and select ***Rotate***. Repeat this or use ***Ctrl-R*** to rotate the TDR probe to the plus sign facing up.
- From the ***Component Libraries*** menu, under ***Nexxim Circuit Elements***, under ***Resistors***, select RES_:Resistor and drag it into the schematic.
- Click a second time to place the second resistor in the circuit.
- Right-click and select ***Place*** and ***Finish*** to place the third resistor.





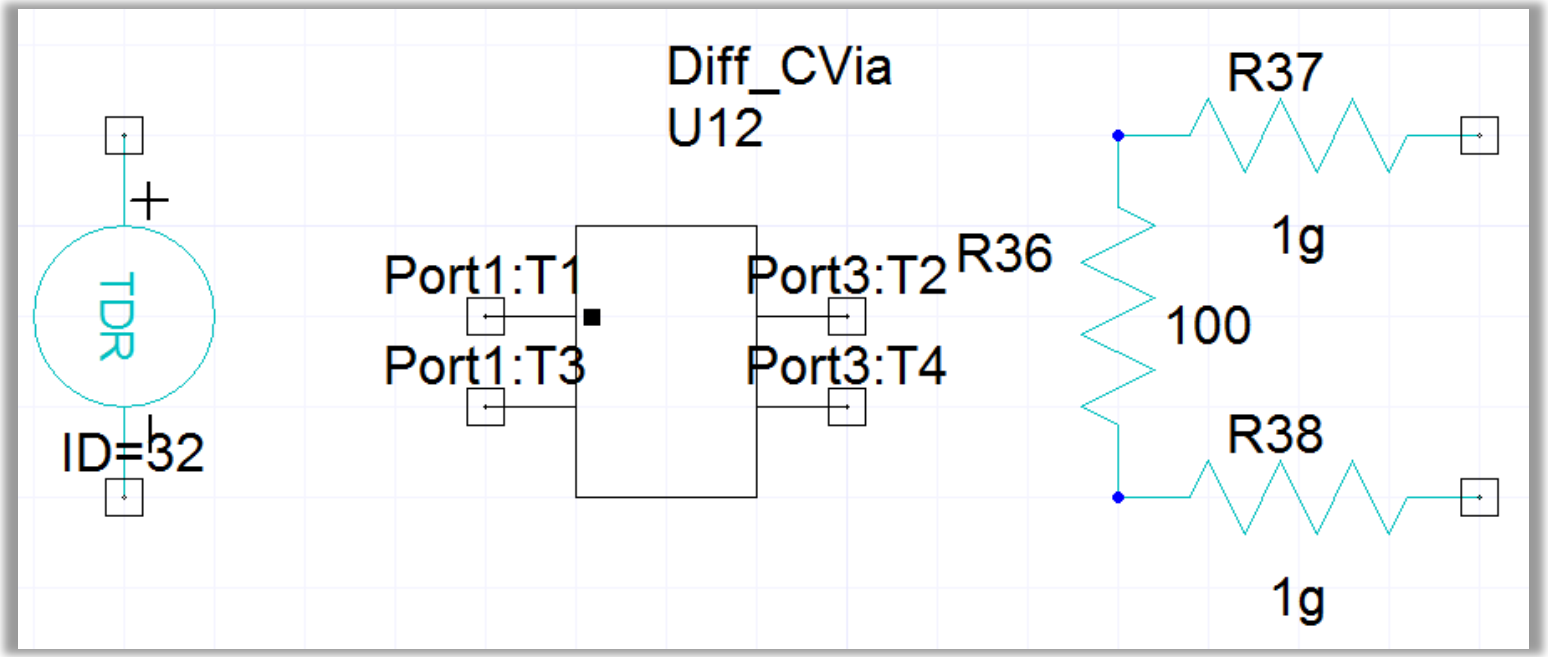
Arrange Resistors and Add Resistor Values to Diff_CVia_TDR1.aedt

Schematic components can be moved by left-click and drag. Components can be rotated by with ***Ctrl-R***. Component values can be changed by double-clicking on the value and editing it.

- Arrange the resistors as shown and assign the value of 100 ohms to the vertical resistor and 1 G ohms to the horizontal resistors.

The schematic reference designators, such as **U12** and **R37** are collectively sequential; the numbers you get may likely be different from the numbers in these slides.

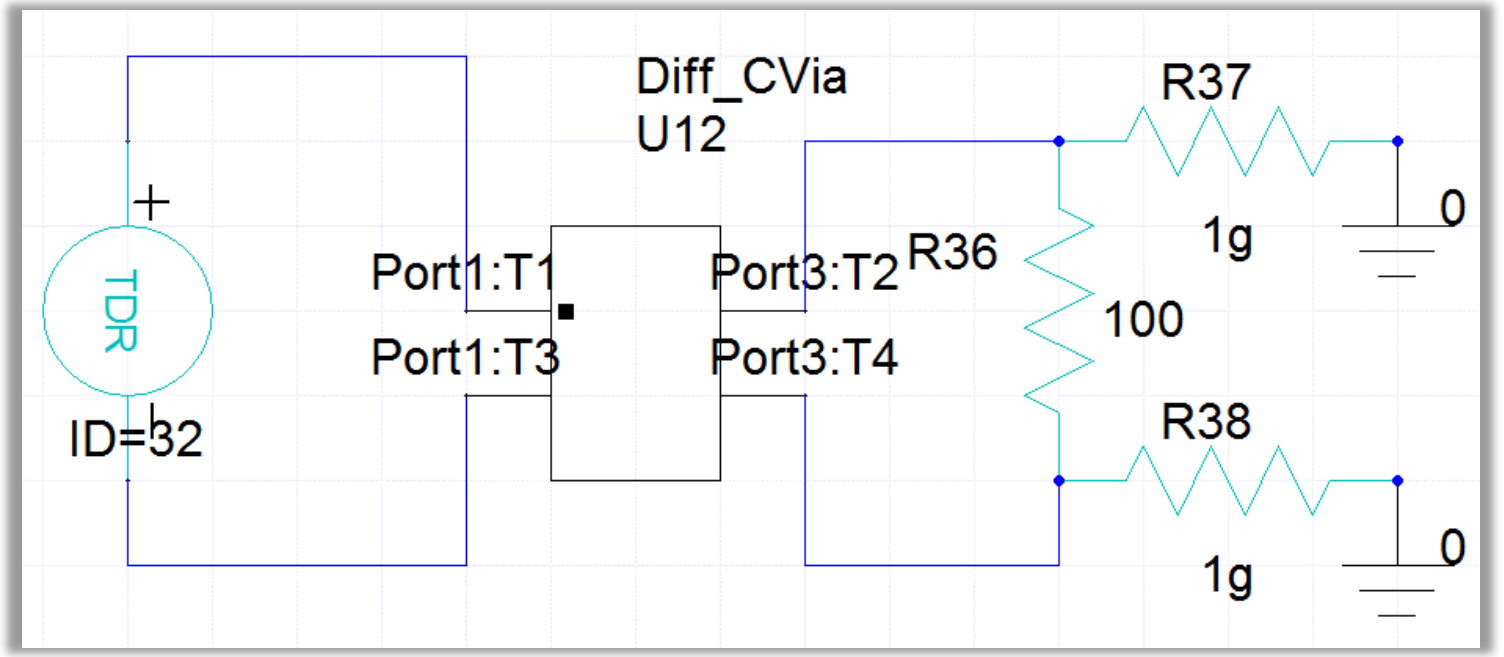
Also note that the labels, such as **1g** and **R38**, can be dragged and repositioned.



Add Grounds and Connect Components - Diff_CVia_TDR2.aedt

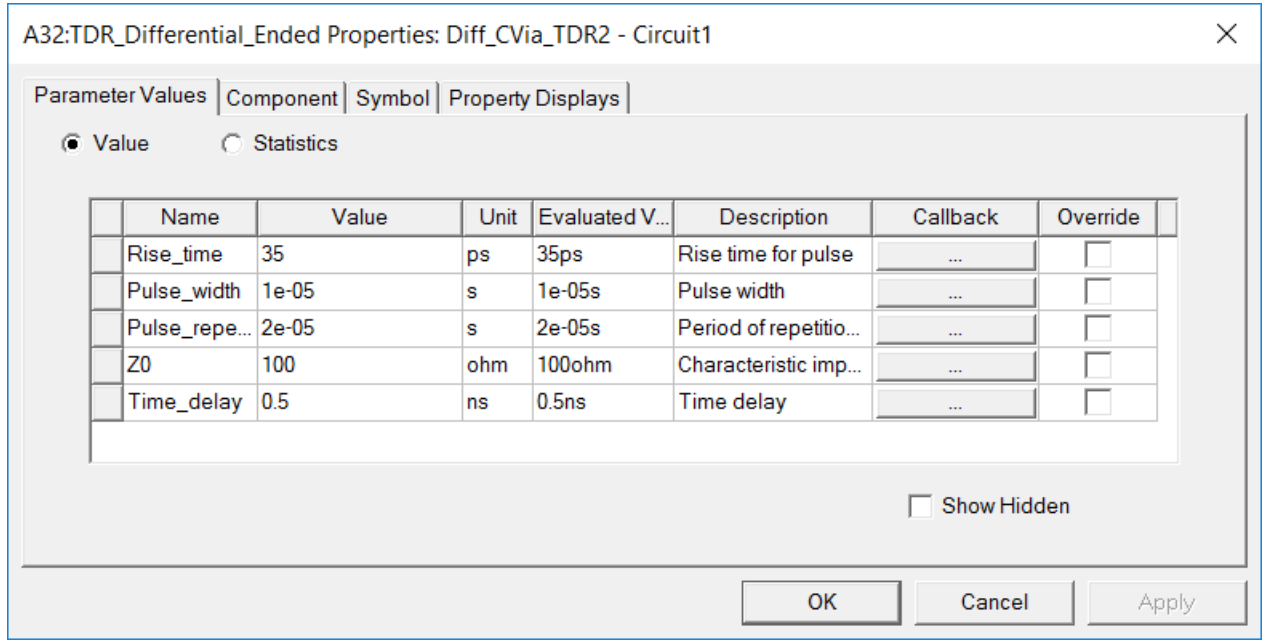
Components can be connected with wires by simply clicking with the mouse on connection points and corners of trace shapes. Ground is available in the Ribbon with the **Schematic** tab selected.

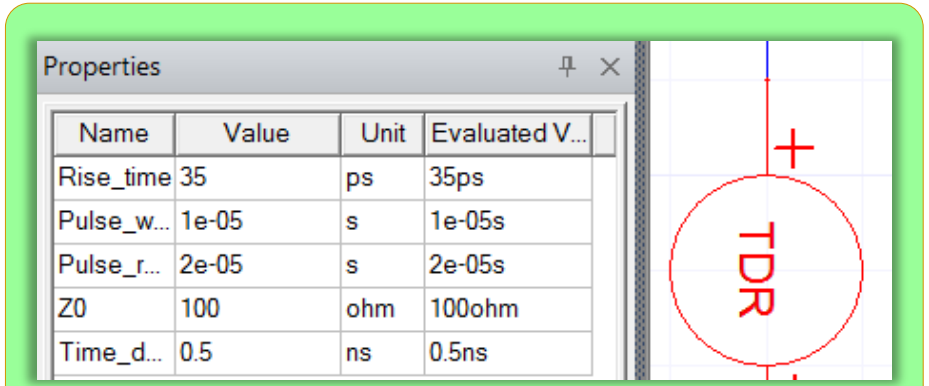
- Connect the schematic elements as shown.
- Add two ground symbols.
- Save As **Diff_CVia_TDR2.aedt**.



Verify TDR Rise Time at 35 ps - Diff_CVia_TDR2.aedt

- Double-click on the TDR schematic component to bring up the ***Properties*** dialog box.
- In the ***Parameter Values*** tab, Verify that the ***Rise_Time*** is set to **35 ps**.
- Click OK to close the ***Properties*** dialog box.



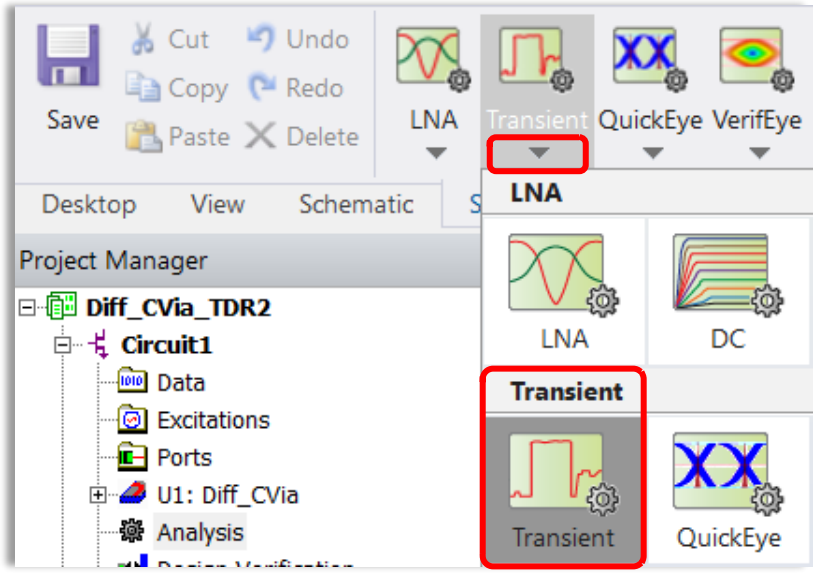


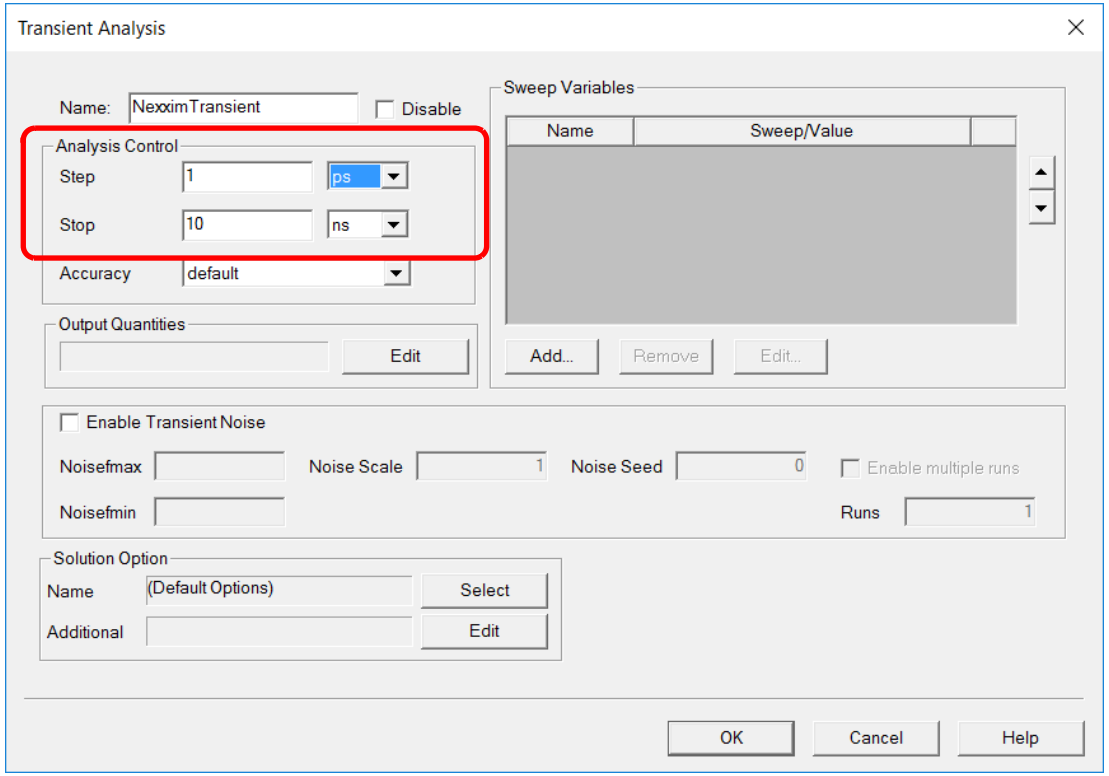
The TDR probe rise time can also be verified and modified in the Properties window.

The rise time can also be parameterized by typing in a variable name and creating a local design variable.

Add Nexxim Solution Setup Transient Analysis

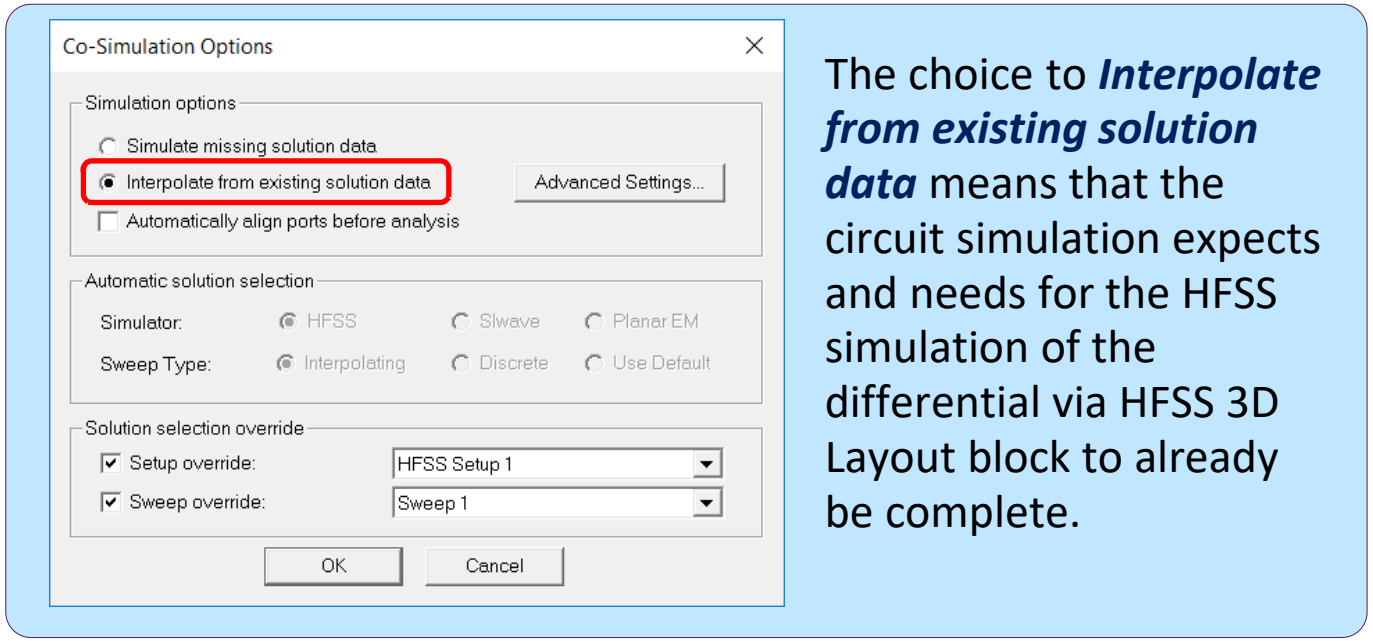
- In the Ribbon, with the **Simulation** tab highlighted, click on the triangle below ***Transient*** and select ***Transient***. This brings up the ***Transient Analysis*** dialog box.
- In the ***Transient Analysis*** dialog box, set the ***Step*** to **1 ps** and verify that the ***Stop*** is **10 ns.**
- Click ***OK*** to close the ***Transient Analysis*** dialog box.



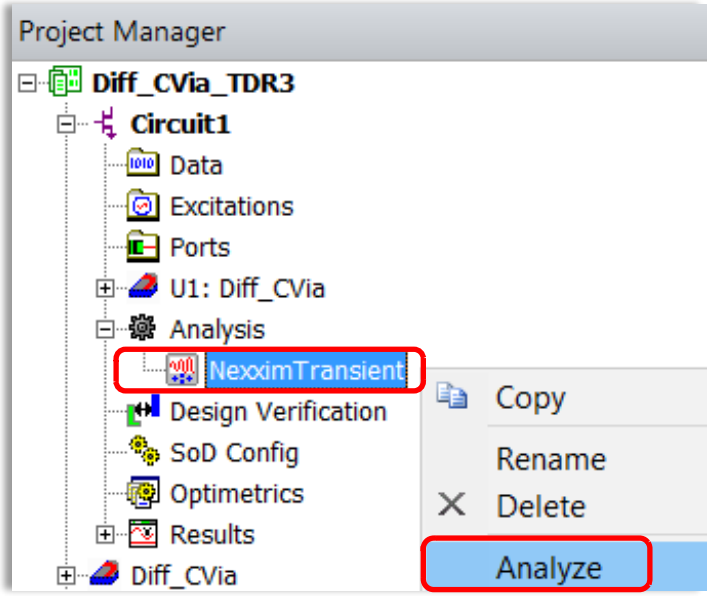


Save to Diff_CVia_TDR3.aedt and aAnalyze - Case 1

- Save project as **Diff_CVia_TDR3.aedt**
- In the ***Project Manager***, under the circuit design (Circuit1), expand ***Analysis*** and right-click next to ***Nexxim Transient*** and select ***Analyze***.
- Save project **Diff_CVia_TDR3.aedt** again after the simulation finishes.



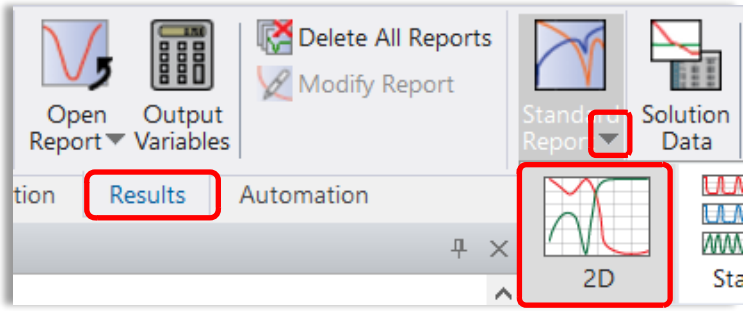
The choice to ***Interpolate from existing solution data*** means that the circuit simulation expects and needs for the HFSS simulation of the differential via HFSS 3D Layout block to already be complete.



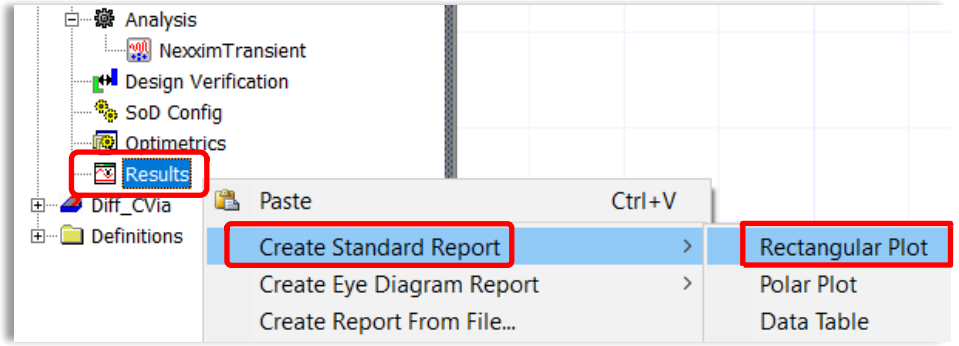
Case 1: long via - stripline on low layer

Open a 2D Results Report

- After the simulation is finished, and with the circuit design selected/highlighted….
- In the ribbon, with the **Results** tab selected, click on the triangle under ***Standard Report*** and select ***2D*** to bring up a 2D ***Report*** specification window.



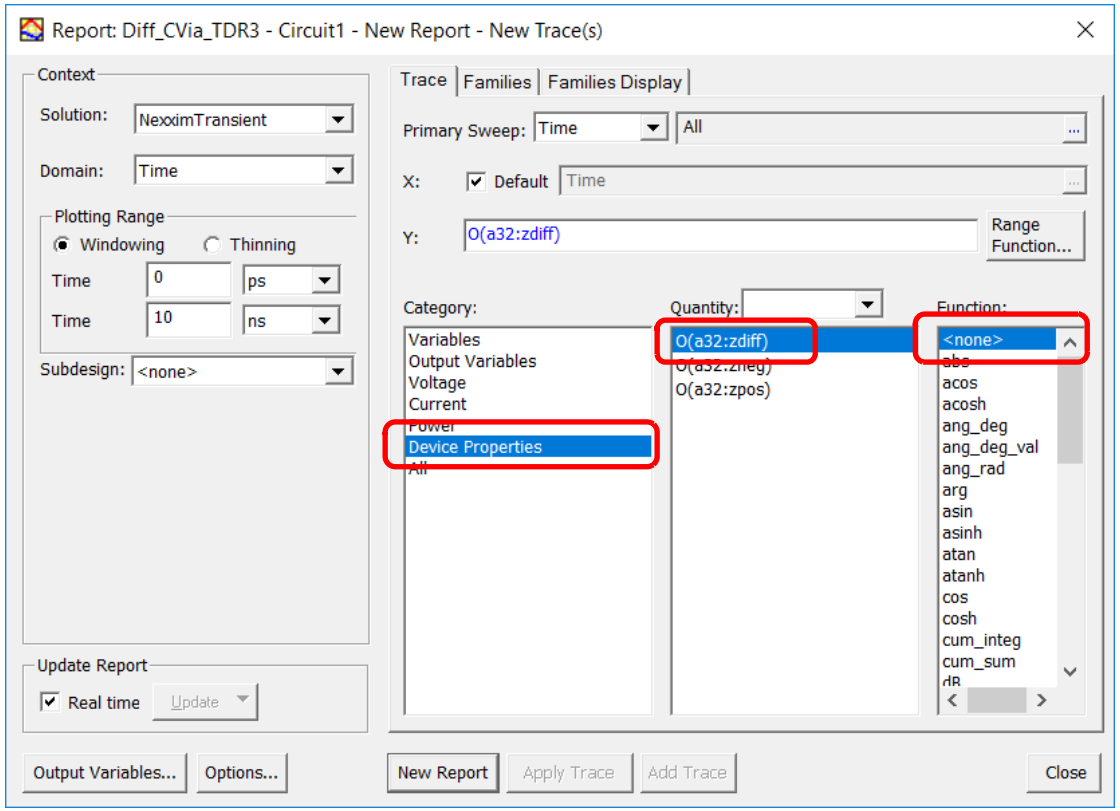
Results Reports can also be generated from within the ***Project Manage***r by right-clicking on ***Results*** and selecting ***Create Standard Report > Rectangular Plot***.



Case 1: long via - stripline on low layer

Plot TDR Response of Differential Via - Diff_CVia_TDR3.aedt

- In this Report setup window choose:
  - ***Category – Device Properties***
  - ***Quantity - O(a32zdiff)***
  - ***Function - <none>***
- Click ***New Report***
- Click ***Close***



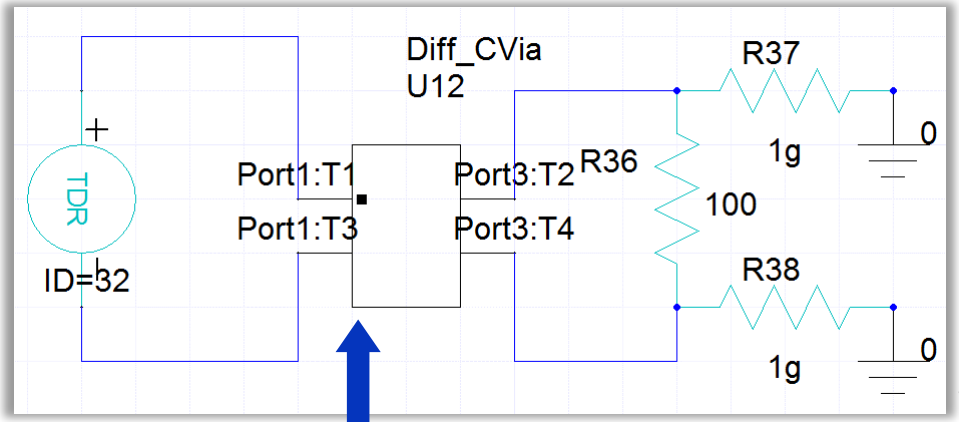
NOTE: the option **O(a32:zdiff)** is characterized by the identification number on the TDR probe in the schematic. It can be different in different projects. Therefore, simply pick the option that has **O(the number that matches the probe you want to plot: zdiff)**.

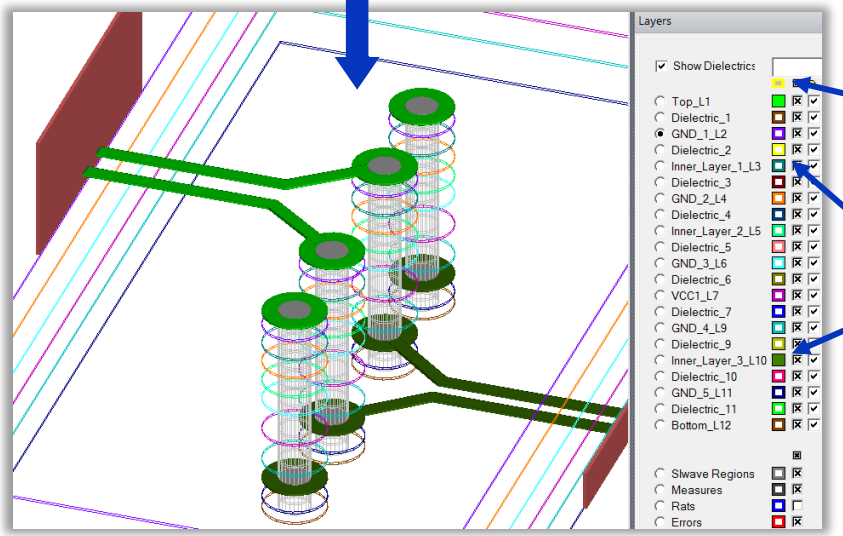
Case 1: long via - stripline on low layer

Case 1 - Diff_CVia_TDR3.aedt - Long Vias to Inner_Layer_3L10

- Case 1 is the differential via with the initial geometry that has the stripline on the lower layer **Inner_Layer_3_L10**.

Hierarchy: The schematic is the top level of hierarchy. The schematic calls circuit element components, like the resistors and the TDR proble. The schematic also calls the differential via EM simulation block like a circuit element.





Viewing Note: The via view has most of the layer set to ***Sketch*** with the ***Fill/Unfill*** setting in yellow unfilled.

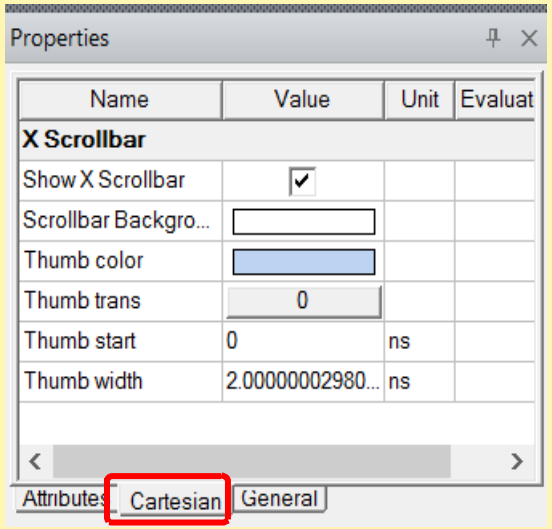
Then the two trace layers are each set to filled.

These ***Layer*** menu settings override a ***Display Solid*** setting.

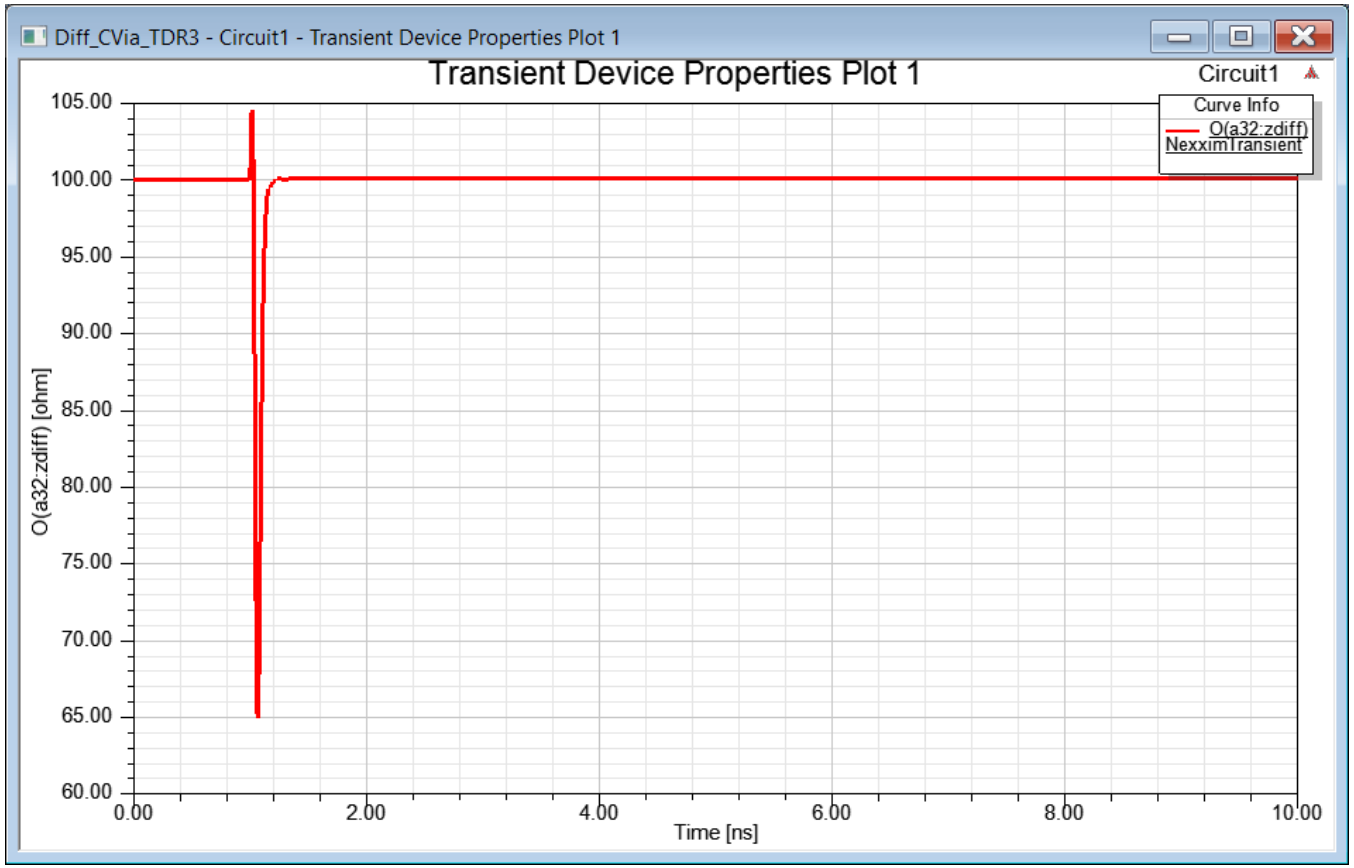
TDR Response of Differential Via - Diff_CVia_TDR3.aedt

Notice how the impedance dips down as far as about 65 ohms from the nominal 100 ohm differential impedance.

- Save project **Diff_CVia_TDR3.aedt**



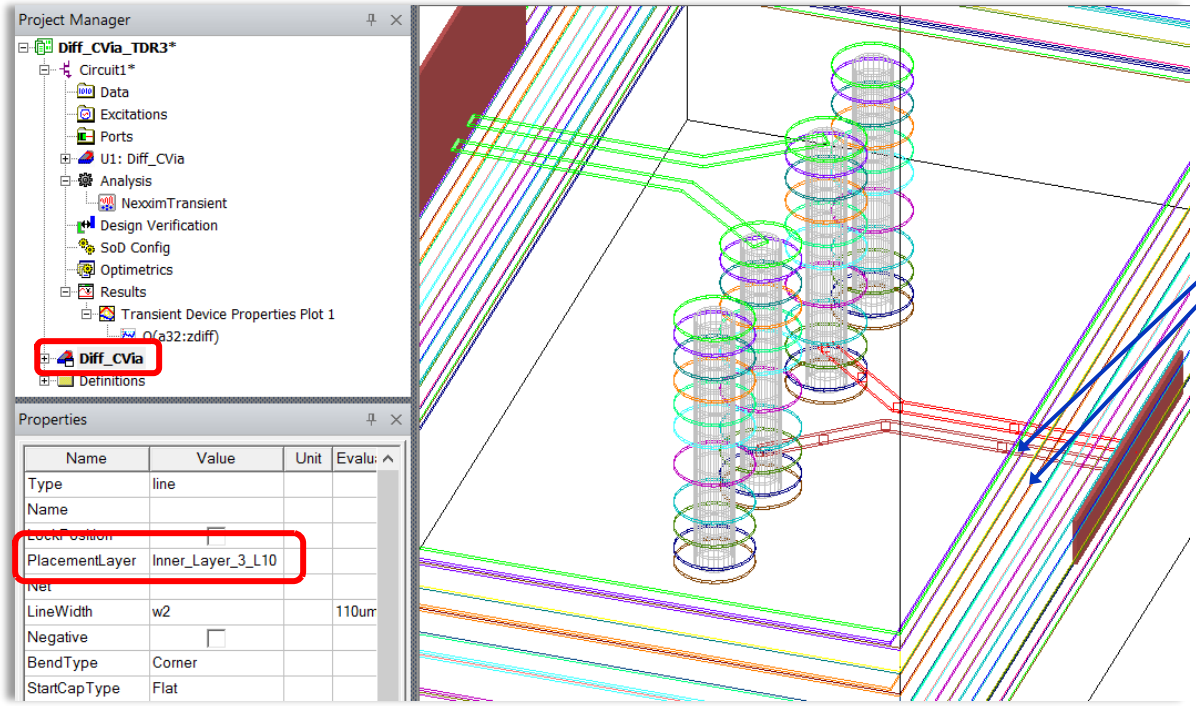
With the trace selected, the X-axis scale can be changed in Properties in the Cartesian tab.



Select Stripline Traces in Diff_CVia_TDR4.aedt

- Save project **Diff_CVia_TDR3.aedt** if not already saved after the plot was made.
- Save the project as **Diff_CVia_TDR4.aedt**.
- In the ***Project Manager***, double-click on the differential pair design **Diff_CVia** to bring it into view.
- Using Ctrl-click select the two stripline traces that sit on the lower layer Inner_Layer_3_L10.

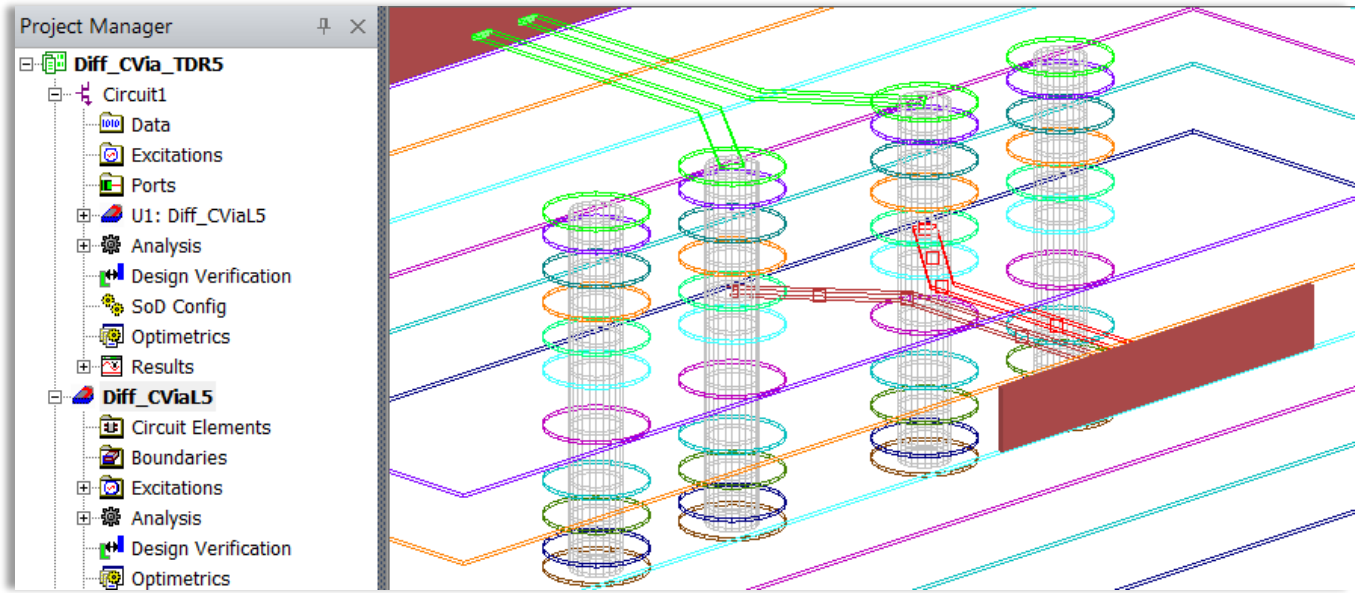
It might be necessary to set ***Display Sketch*** in the ribbon or in the ***Layers*** menu to make the selection of the traces below other layers. The "B" key also selects what is behind a shape where one clicks.

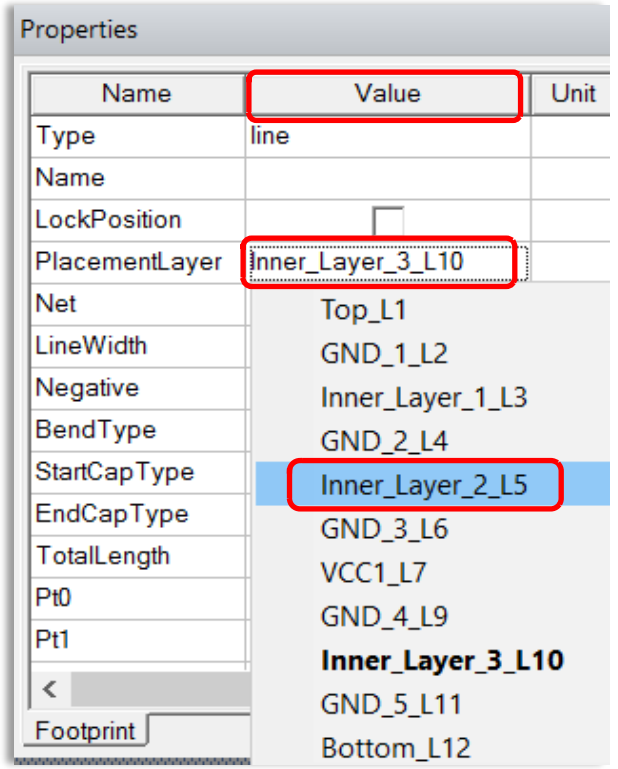


The two selected stripline traces on Inner_Layer_3_L10. The red one was selected first.

Move Stripline Traces to Higher Layer - Diff_CVia_TDR5.aedt

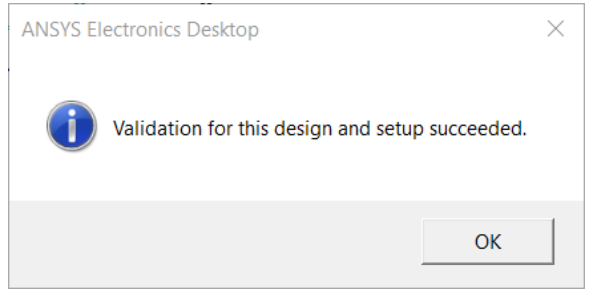
- In the ***Properties*** menu, (with the stripline traces still selected), click on the ***PlacementLayer Value*** to invoke a drop down menu of layers in the via design.
- Select **Inner_Layer_2_L5**
- In the ***Project Manager***, right-click on the differential via design **Diff_CVia** and change its name to **Diff_CViaL5**.
- Save the project as **Diff_CVia_TDR5.aedt**.





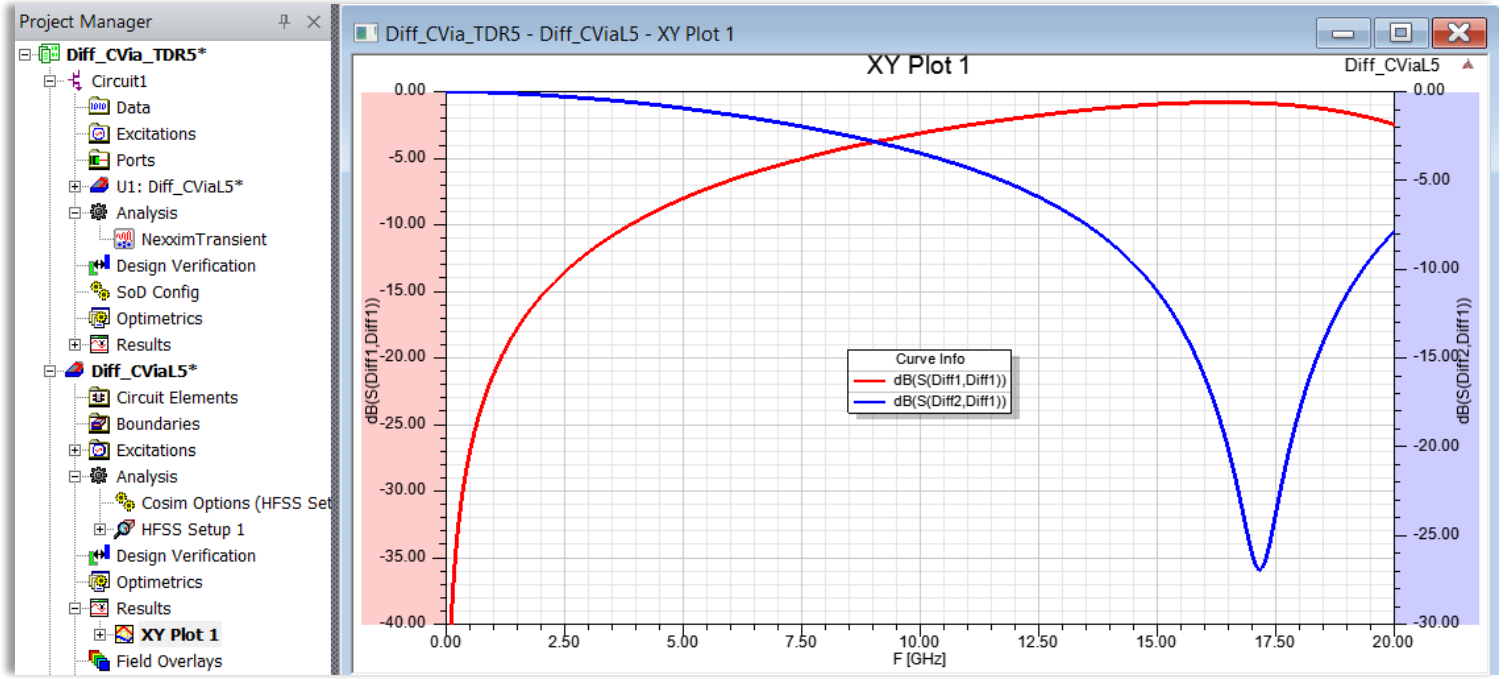
Simulate Diff_CViaL5 HFSS Setup 1 - Case 2

- In the ***Project Manager***, under the **Diff_CViaL5** design, under ***Analysis***, right-click on the **HFSS Setup 1** and select ***Validate***.
- After validation, right-click again on ***HFSS Setup 1*** and select ***Analyze.***
- When the simulation finishes, save the project **Diff_CVia_TDR5.aedt**.



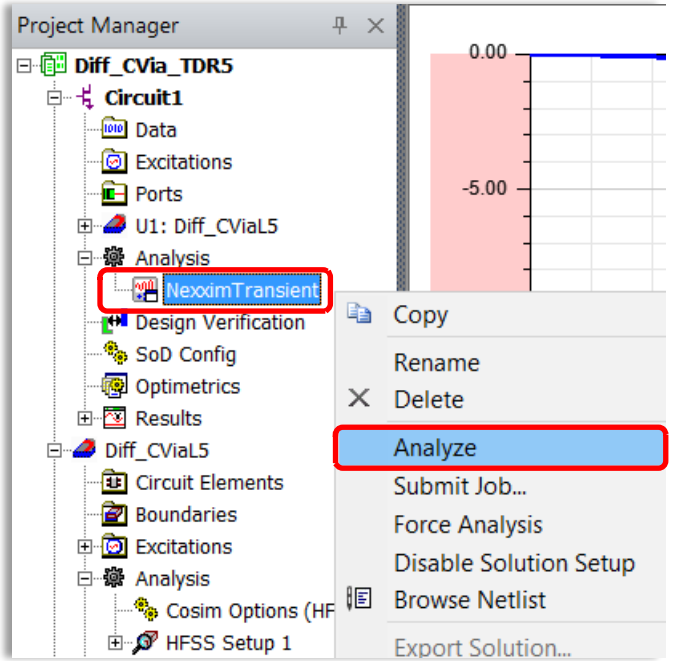
Notice the distinct resonance in the transmission and corresponding deterioration in reflection between 15 and 18 GHz.

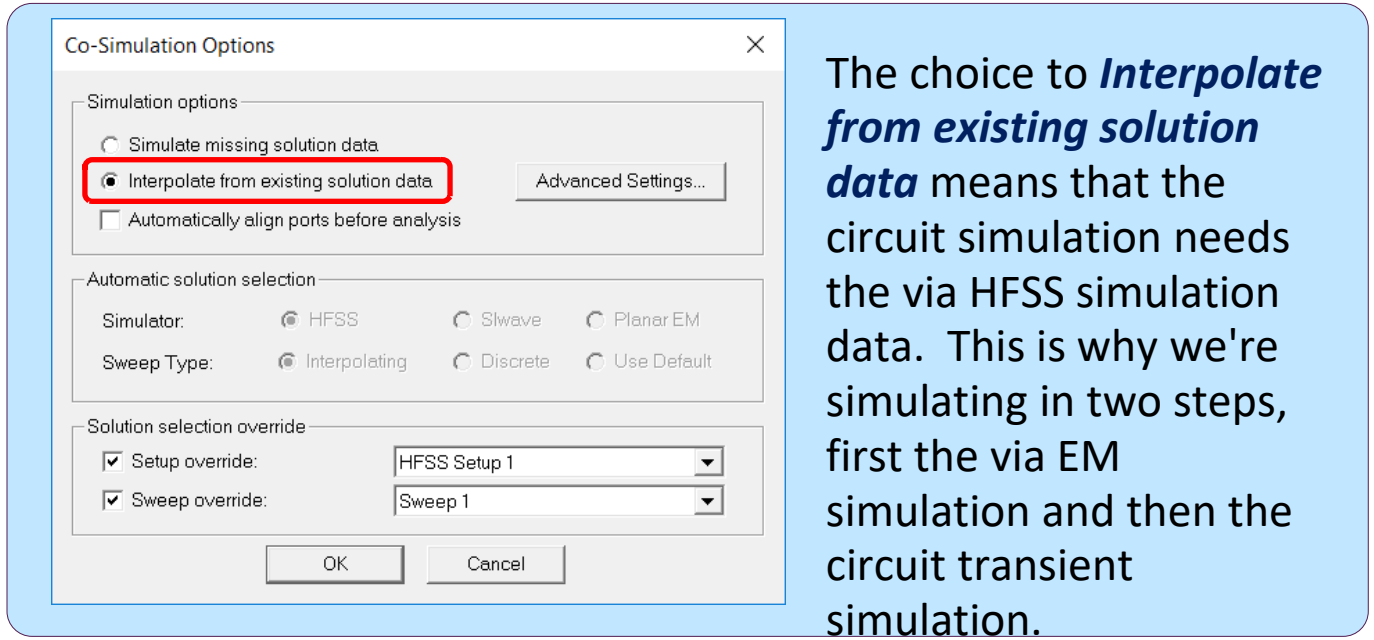
The asterisks * on the project name and the design name **Diff_CViaL5** indicate that the project was not yet saved when the screen shot was made.



Simulate Circuit1 *Nexxim Transient*

- In the ***Project Manager***, under the circuit design, under Analysis, right-click on Nexxim Transient and select Analyze.
- When the simulation finishes, save the project **Diff_CVia_TDR5.aedt**.
- In the ***Project Manager***, Under ***Results***, double-click on the **Transient Device Properties Plot 1** to bring the updated plot into view.



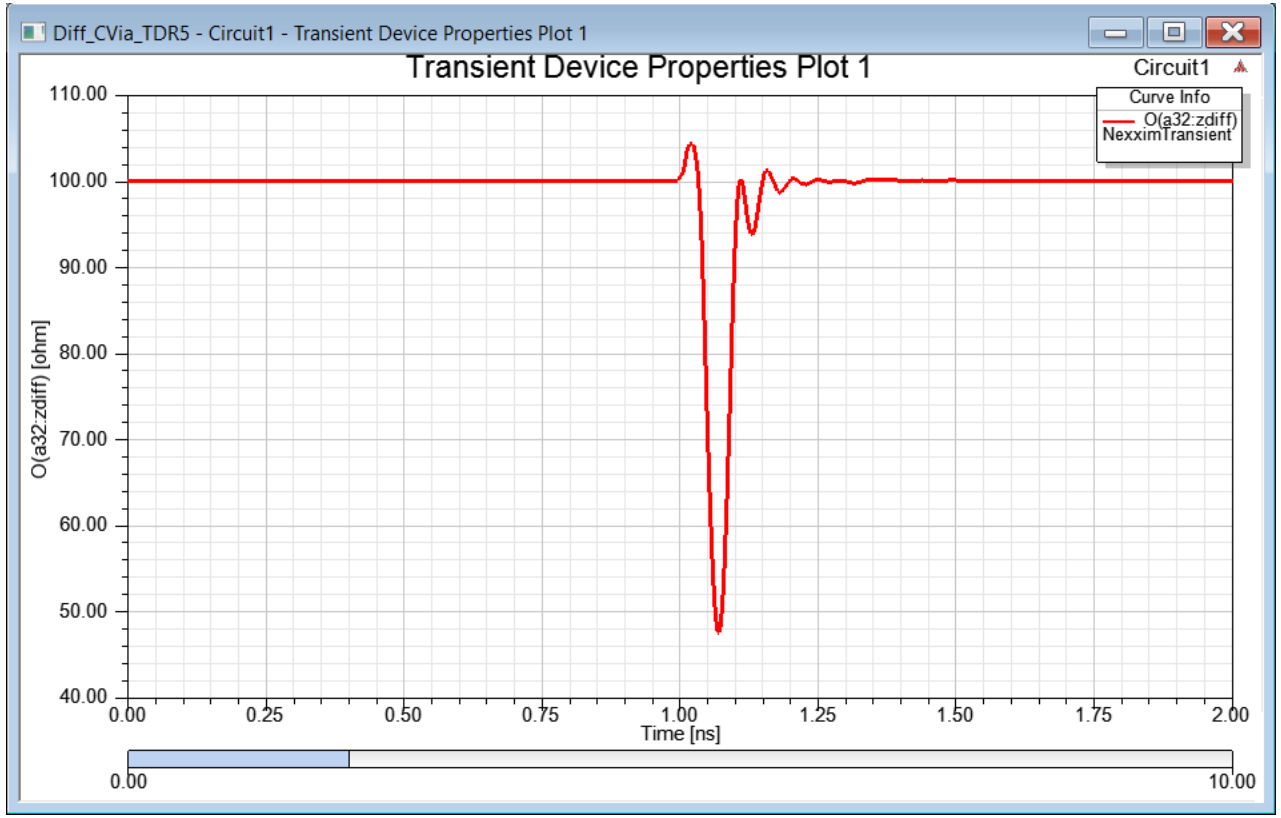


The choice to ***Interpolate from existing solution data*** means that the circuit simulation needs the via HFSS simulation data. This is why we're simulating in two steps, first the via EM simulation and then the circuit transient simulation.

Larger Impedance Dip Higher in Diff_CVia_TDR5.aedt - Case 2

- Click on the red signal trace itself in the plot to select.
- Click on the Cartesian tab.
- Click the box ***Show X Scrollbar.***
- Change Thumb width to 2 ns (from 10 ns.)

For this simulation, with the stripline traces on **Inner_Layer_2_L5**, notice that the shape of the TDR response is similar to before, but the impedance dips below 50 ohms, lower than the first simulation with the stripline on the lower layer **Inner_Layer_3_L10**. The structure now has a significant via stub below **Inner_Layer_2_L5.**

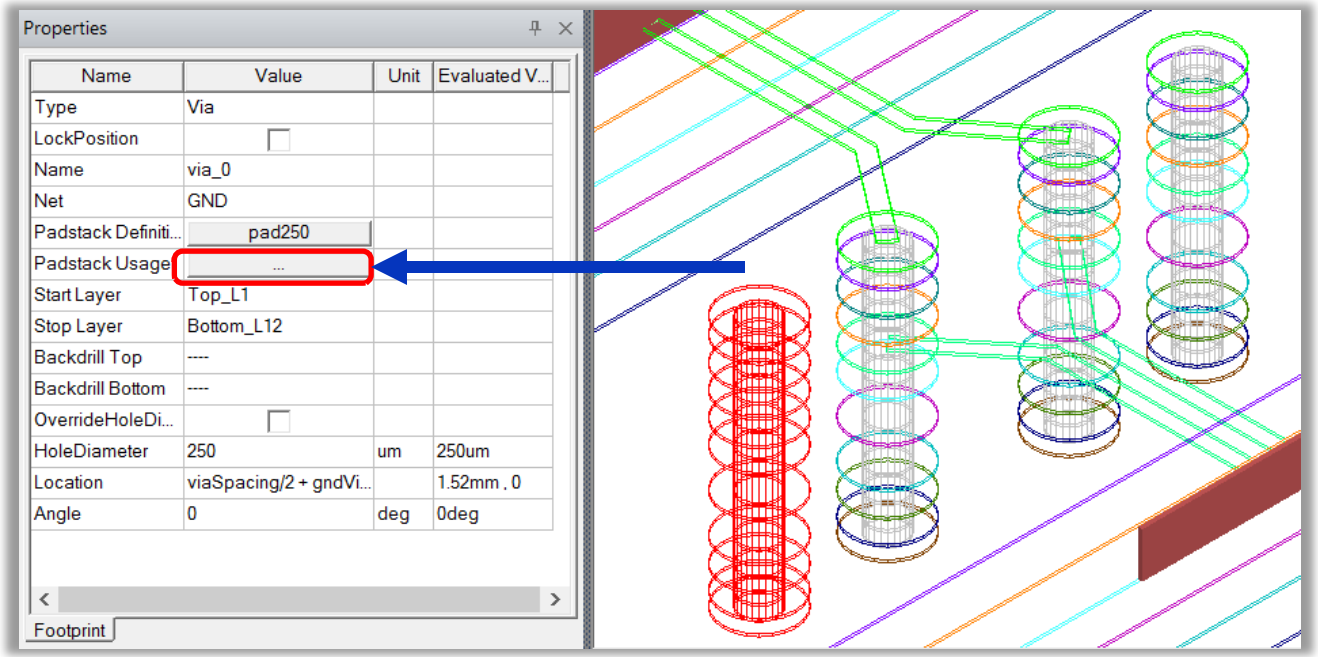


Open Padstack Usage and Definition for First Via

- Save the project as **Diff_CVia_TDR6.aedt.**
- In the ***Project Manager*****,** double-click on the differential pair design **Diff_CViaL5** to bring it into view.
  In the ribbon Layout tab Orient > Isometric gives us a good view.
- Select one via as shown below. (via_0 is highlighted in red.)
- In the ***Properties,*** under ***Padstack Usage,*** click on the button under Value, that shows …

…to bring up the ***Padstack Usage and Definition*** dialog box.

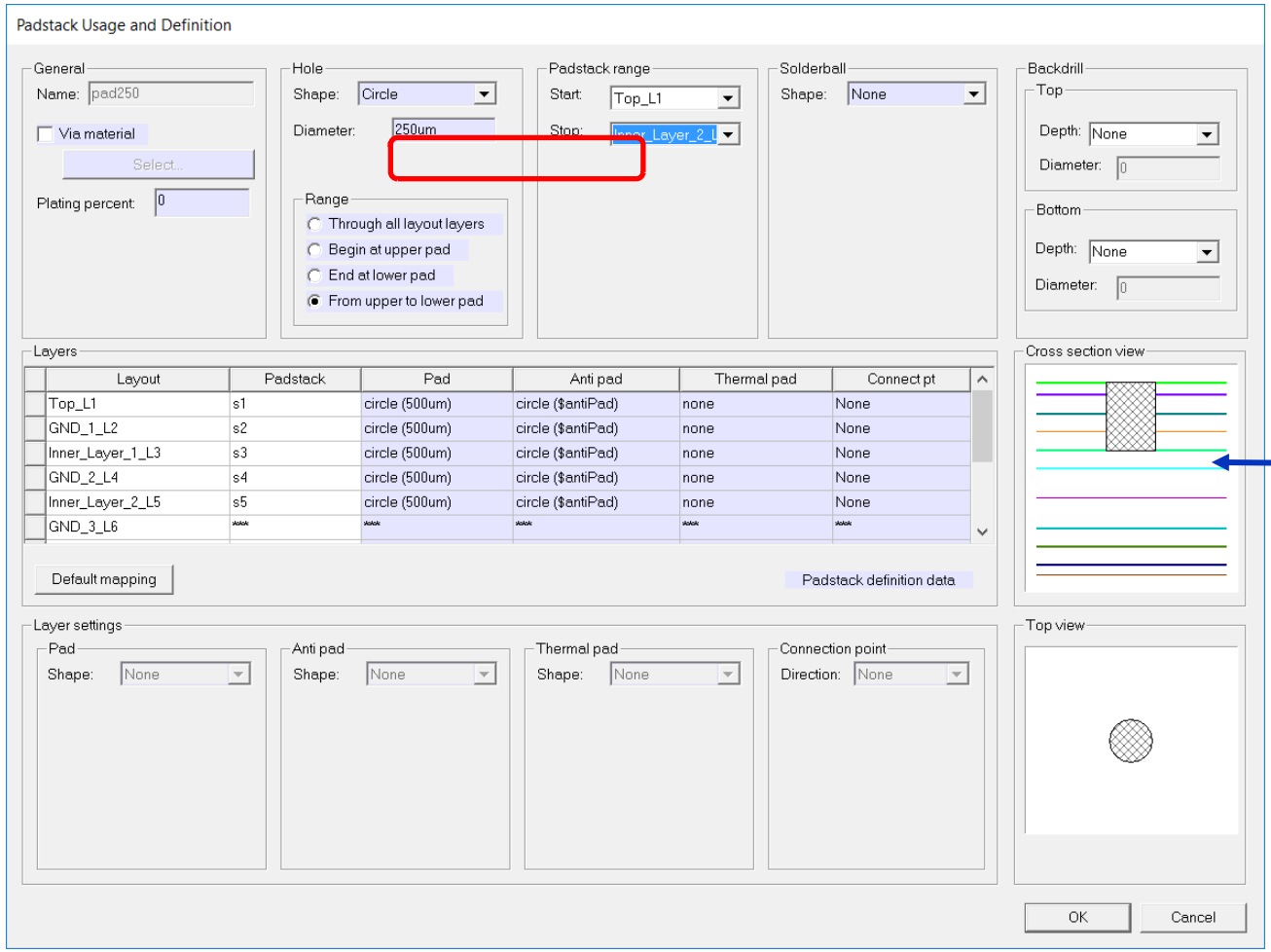
Diff_Cvia_TDR6.aedt



Open Padstack Usage and Definition for First Via

- In the upper middle, Under ***Padstack range***, change the ***Stop***: to **Inner_Layer_2_L5.**
- Click ***OK*** to close the ***Padstack Usage and Definition*** dialog box.

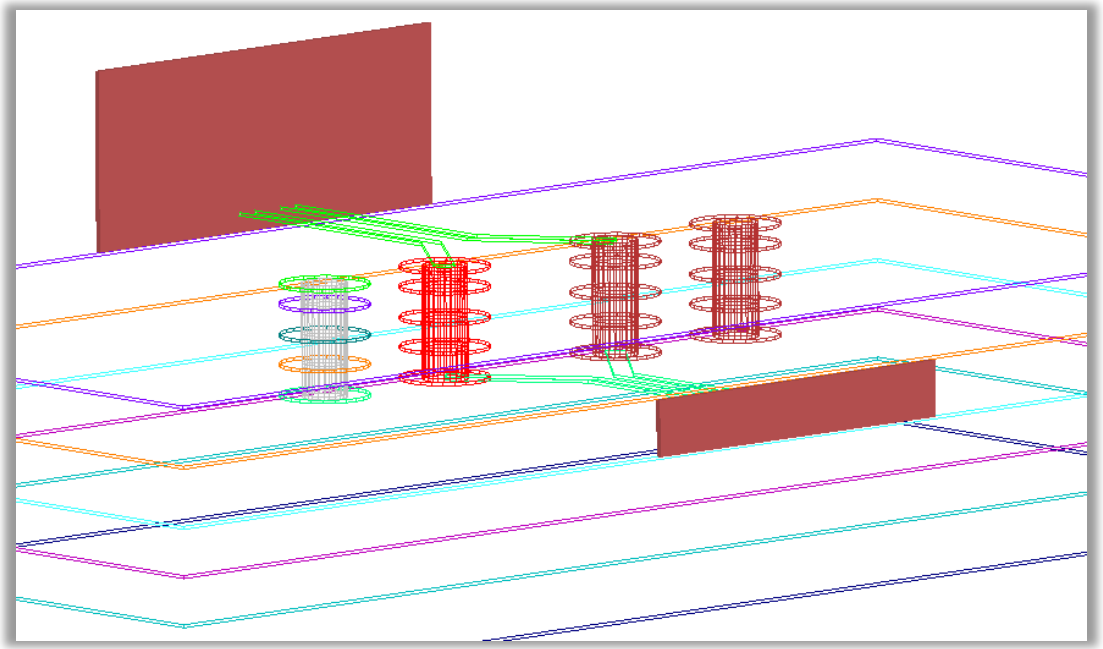
Diff_Cvia_TDR6.aedt

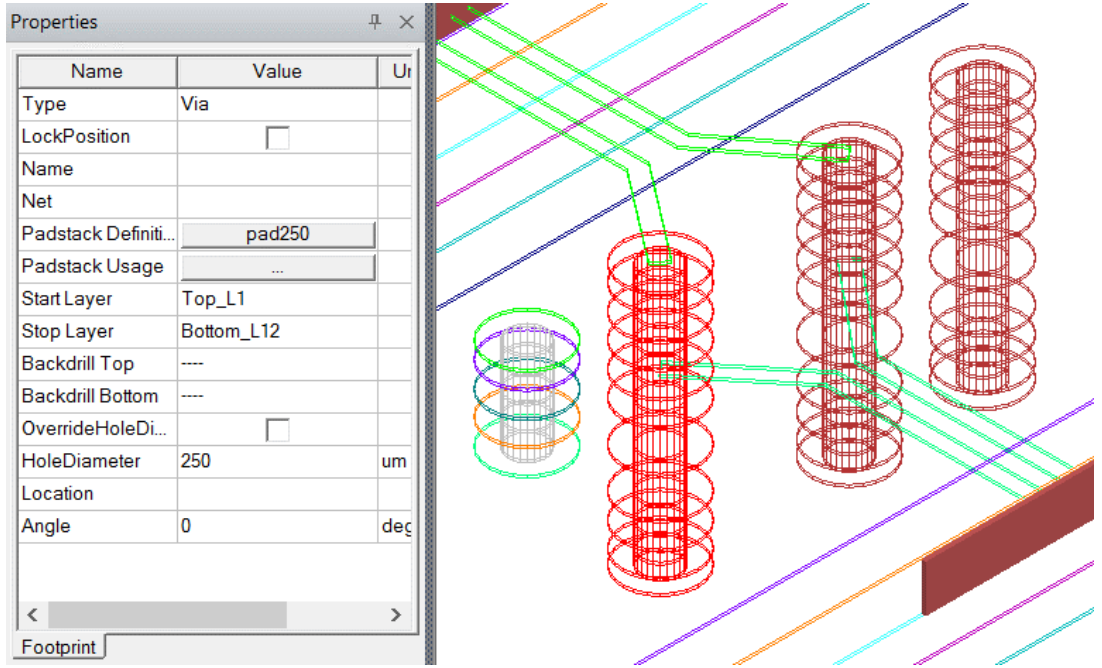


This shows the shorter cross section of the new via size after we change the stop layer.

Adjust Padstack Range to *Inner_Layer_2_L5* on 3 Vias - Case 3

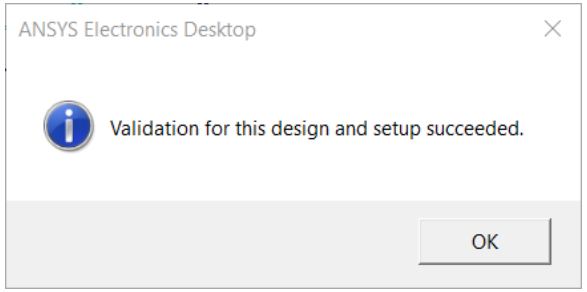
- Using Ctrl-click, Select all three remaining vias.
- Repeat process of opening up the ***Padstack Usage and Definition*** dialog box and changing the ***Padstack range Stop***: to **Inner_Layer_2_L5**.
- In the ***Project Manager***, right-click on the differential via design **Diff_CViaL5** and change its name to **Diff_CViaL5_BD**.
- Save the project **Diff_CVia_TDR6.aedt**.





Simulate Diff_CViaL5_BD HFSS Setup 1 in Diff_CVia_TDR6.aedt

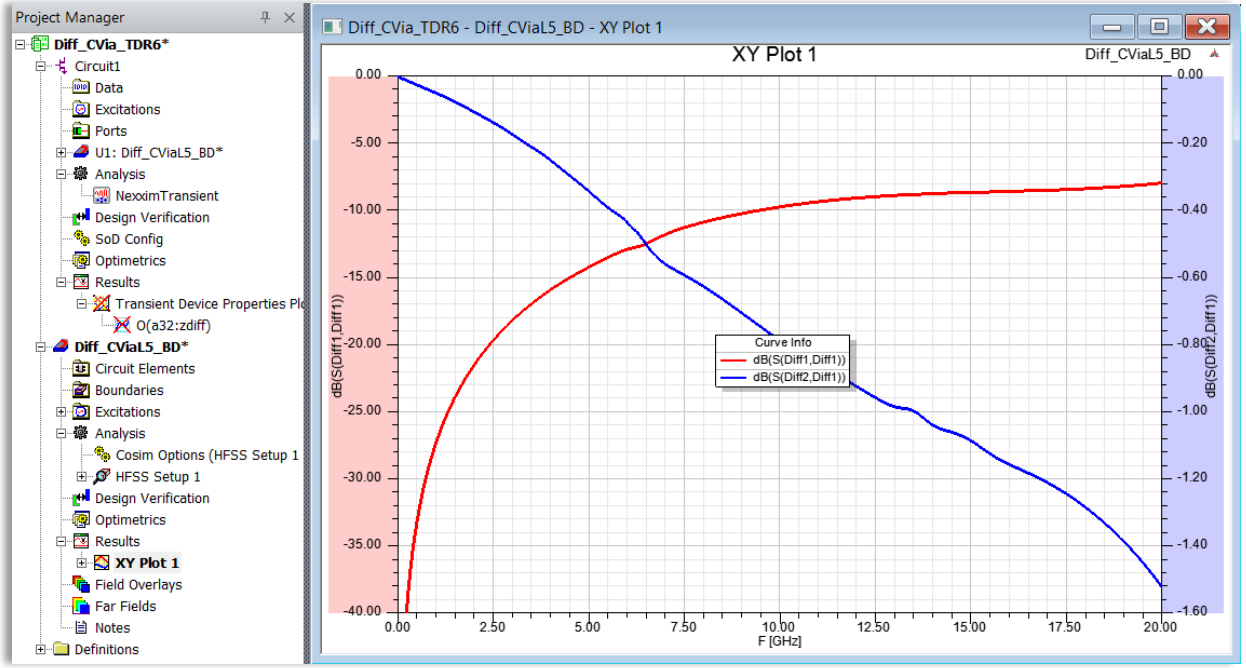
- In the ***Project Manager***, under the **Diff_CViaL5_BD** design, under ***Analysis***, right-click on the **HFSS Setup 1** and select ***Validate***.
- After validation, right-click again on ***HFSS Setup 1*** and select ***Analyze.***
- When the simulation finishes, save the project **Diff_CVia_TDR6.aedt**.



We no longer have the distinct resonance in the transmission and corresponding deterioration in reflection between 15 and 18 GHz.

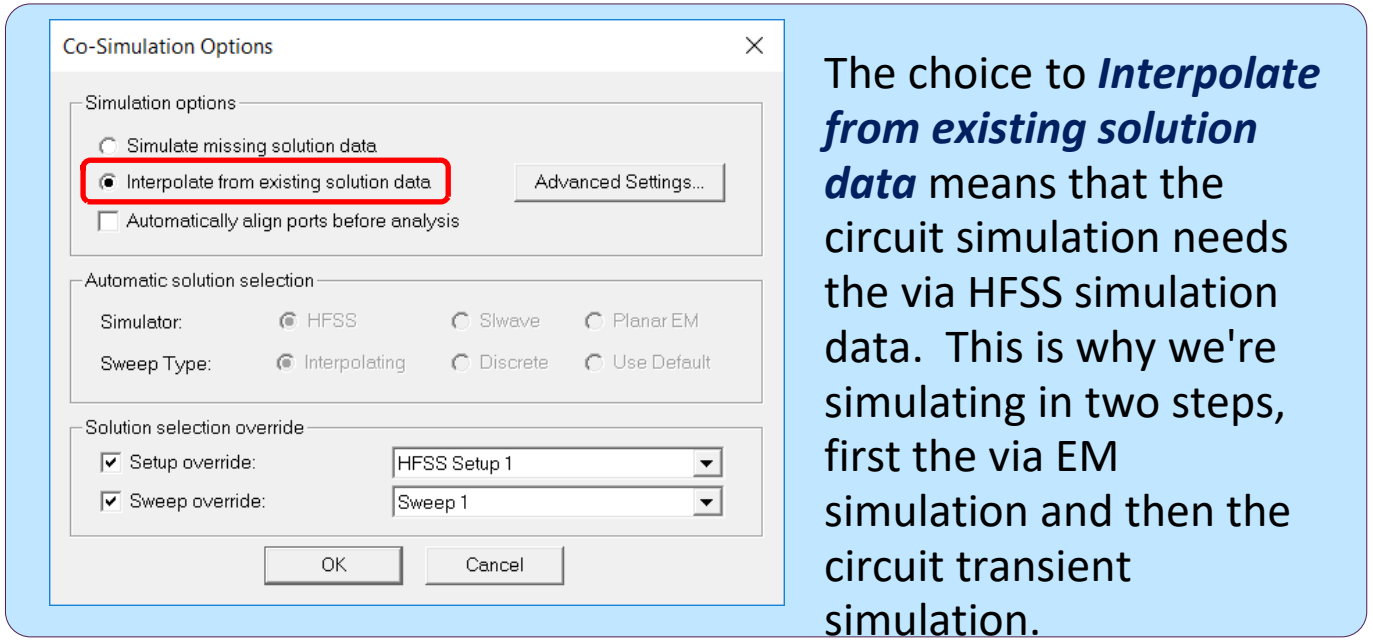
Also notice how the transient circuit analysis results have red Xs through them, indicating that they're invalid (until we resimulate).

Case 3

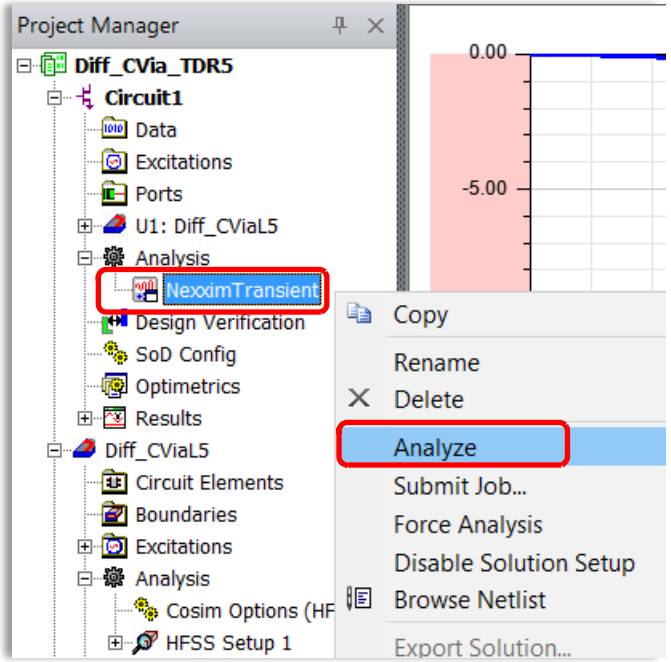


Simulate Circuit1 *Nexxim Transient* - Diff_CVia_TDR6.aedt

- In the ***Project Manager***, under the circuit design, under Analysis, right-click on Nexxim Transient and select Analyze.
- When the simulation finishes, save the project **Diff_CVia_TDR6.aedt**.
- In the ***Project Manager***, Under ***Results***, double-click on the **Transient Device Properties Plot 1** to bring the updated plot into view.



The choice to ***Interpolate from existing solution data*** means that the circuit simulation needs the via HFSS simulation data. This is why we're simulating in two steps, first the via EM simulation and then the circuit transient simulation.

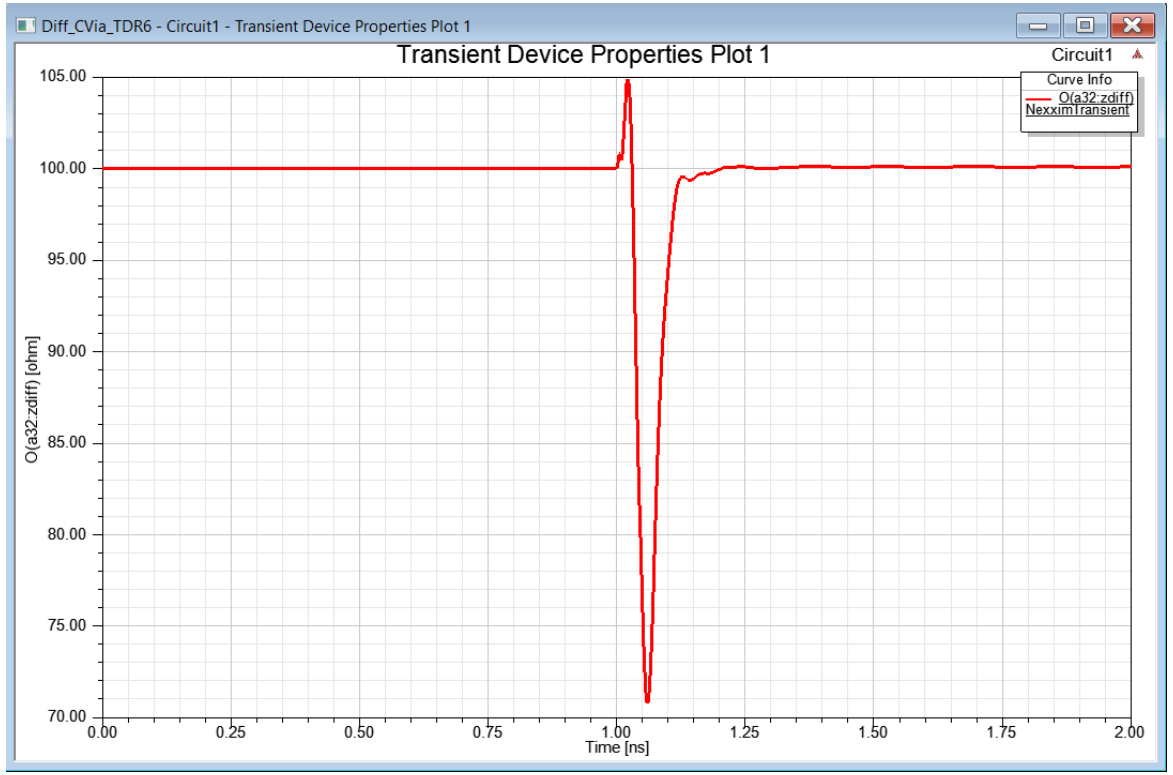


Case 3: via stub removed in padstack usage

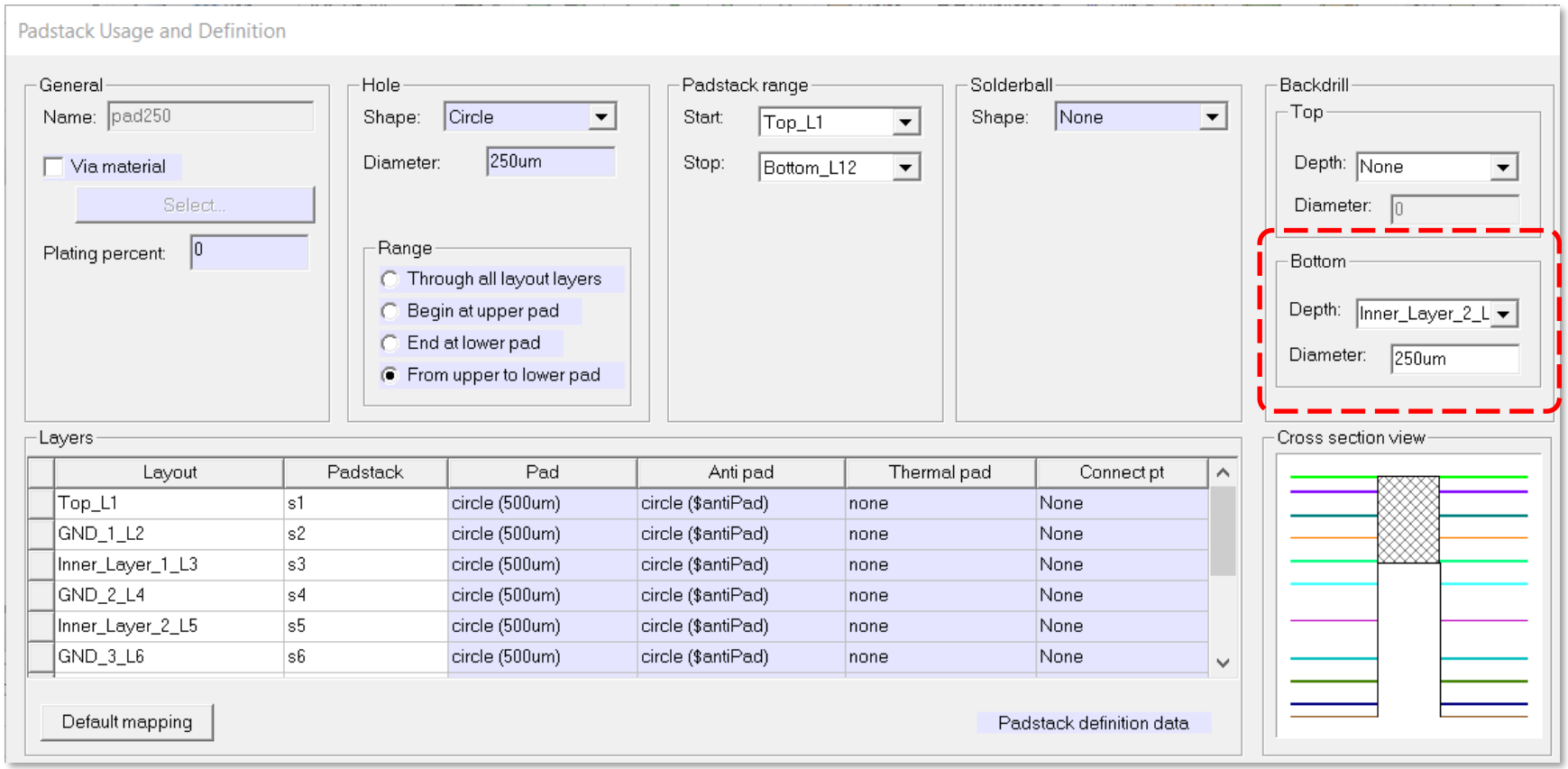
Larger Impedance Dip Higher in Diff_CVia_TDR6.aedt - Case 3

- Click on the red signal trace itself in the plot to select.
- Click on the Cartesian tab.
- Click the box ***Show X Scrollbar.***
- Change Thumb width to 2 ns (from 10 ns.)
- Uncheck the box ***Show X Scrollbar.***

For this simulation, with the stripline traces on **Inner_Layer_2_L5** and the via stub removed, notice that the impedance dips to almost 70 ohms, slightly better than the first simulation with the stripline on the lower layer **Inner_Layer_3_L10**.



Optional - Compare Backdrill to *Inner_Layer_2_L5* on 3 Vias



Notice how the ***Cross section view*** reflects the ***Backdrill*** settings and the ***Padstack range*** is set back to the full length.


Ansys